

Instruction Manual

Expansion Unit Type 5765

CPC-E-1902



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Brüel & Kjær

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CONTENTS

	No. of pages.
Section 1 Introduction	4
- 2 Description	13
- 3 Operation	3
- 4 Adjustment Procedure	6
- 5 2131 Modifications	2
- 6 Specifications	4
- 7 Parts List	7

DIAGRAMS

Third Octave Filters	WI 0941 to WI 0949
Logarithmic RMS Detector	WI 0950
Inp. Amp. & Power Reg. Circuits	WI 0951, 52, 53, 56
Digital Control I	WI 0954
Digital Control II	WI 0955
Avg. Time & Freq. Range Control	WI 0957, 58.
Component Location Diagram	
Wiring Diagram	

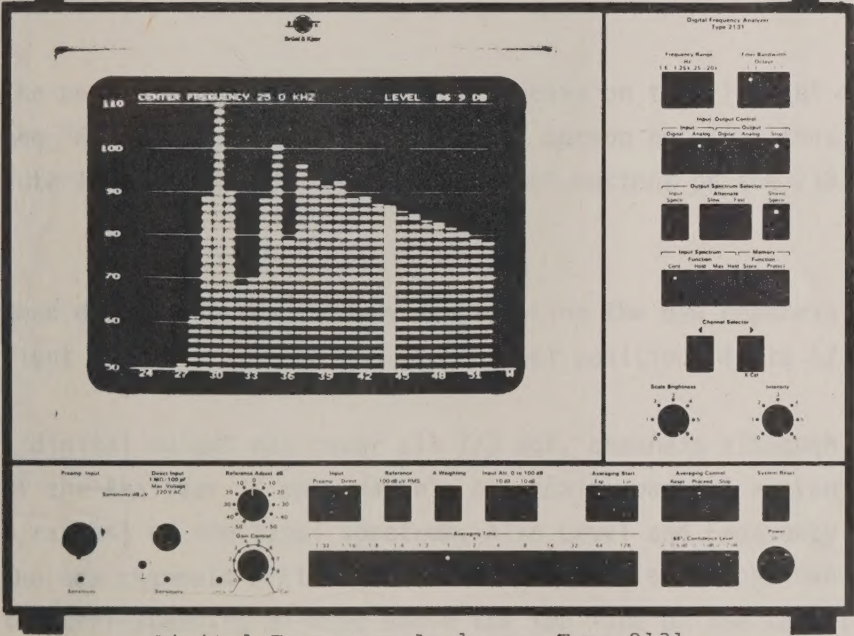


Expansion Unit Type 5765



25kHz - 160kHz

1/3 oct.
channels



1.6 Hz - 20kHz

Digital Frequency Analyzer Type 2131

Intensified column indicates first channel of the 5765 Expansion Unit.



Expansion Unit Type 5765

1. Introduction

The Expansion Unit Type 5765 is an auxiliary instrument for the Digital Frequency Analyzer Type 2131, making it possible to increase the 1/3 oct. analysis range beyond the 20 kHz limit of the standard Analyzer.

In its standard version the 5765 contains nine 1/3 oct. channels with centre frequencies ranging from 25 kHz to 160 kHz. The extended Analyzer System thus covers the 1,6 to 160 kHz analysis range (total: 51 1/3 oct. channels).

The new channels are entered for display on the 2131 CRT on command from the "Freq. Range (200 Hz - 160 kHz)" button on 5765 (this button is interlocked with the two "Freq. Range" buttons on the 2131).

When displayed, the columns representing the new channels are shown to the right of the 20 kHz column (in channel positions 44 to 52).

A digital output may cover all 1/3 oct. channels although the CRT display of the Analyzer is only capable of showing partial extracts (divided in 3 ranges) of the total spectrum, Also Level and Frequency information for the new channels will be available (when selected by Channel Selector) in the corresponding windows above the top line on the CRT, for either selected display range.

The new channels, however, will be excluded from display or readout if the Analyzer is set to "Octave" mode of operation or if the "A-weighting" button is enabled.

In contrast to the filters of the 2131 itself, which are based on digital principles, the filters contained in the Expansion Unit must be analog, as the high sampling rate necessary for digital filtering at these frequencies would be inconsistent with the 2131 processing circuitry.



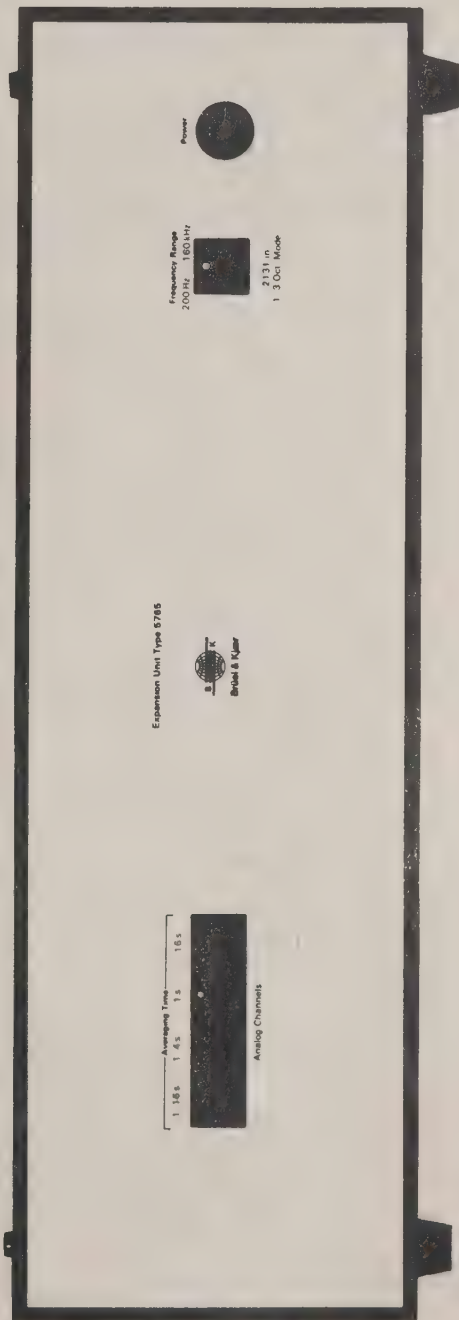
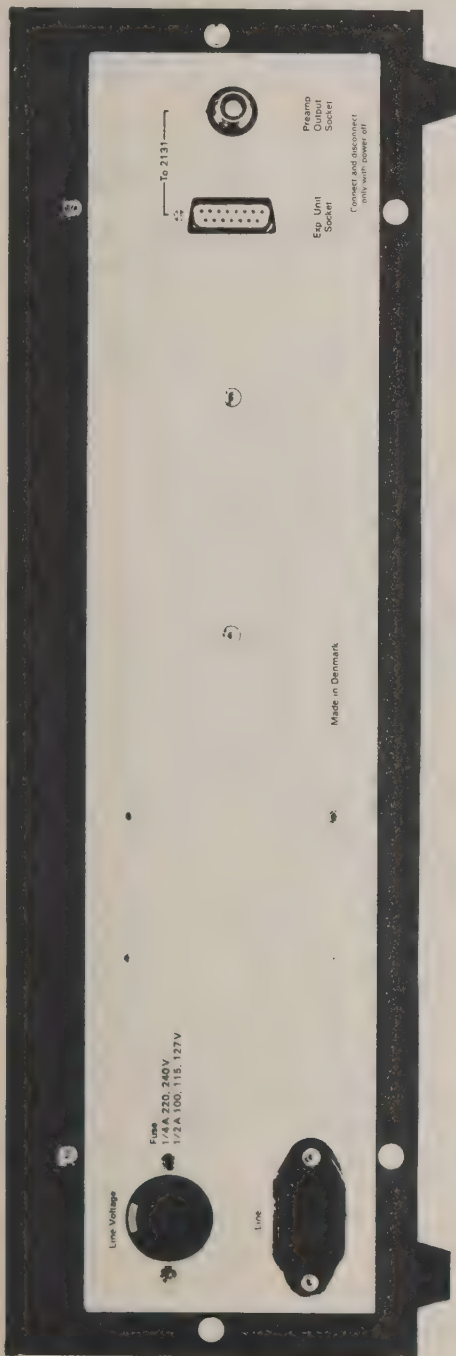
The necessity for analog filtering and RMS detection in the Expansion Unit means, that the following 2131 control features are not active for the new channels:

Averaging Time: 4 different Avg. times for the channels contained in the Expansion Unit may be selected from front panel of the instrument.

Lin. Averaging: The analog channels will not participate in the linear averaging process, but will be continuously updated.

The Expansion Unit is designed to accommodate two further analog channels in addition to the nine standard channels. The two optional channels will be shown in the two rightmost column positions on the CRT (ch 53, 54), which are entered for display for either selected "Frequency Range".

If required, the high frequency 1/3 oct. filters may also be exchanged with other filters on special request.



Front and Rear Panels of the Expansion Unit.



2. Description

General:

The Expansion Unit is connected to the 2131 Analyzer via two sockets on the rear panel of the instrument.

The input signal for the filter bank in 5765 is fed through the coax cable connected to the "Preamplifier Output" socket of 2131, while the mutual control and communication between the two instruments takes place via the connection cable to the 15 pin "Expansion Unit" socket of 2131.

Fig. 2.1 shows the Block Diagram for the Expansion Unit.

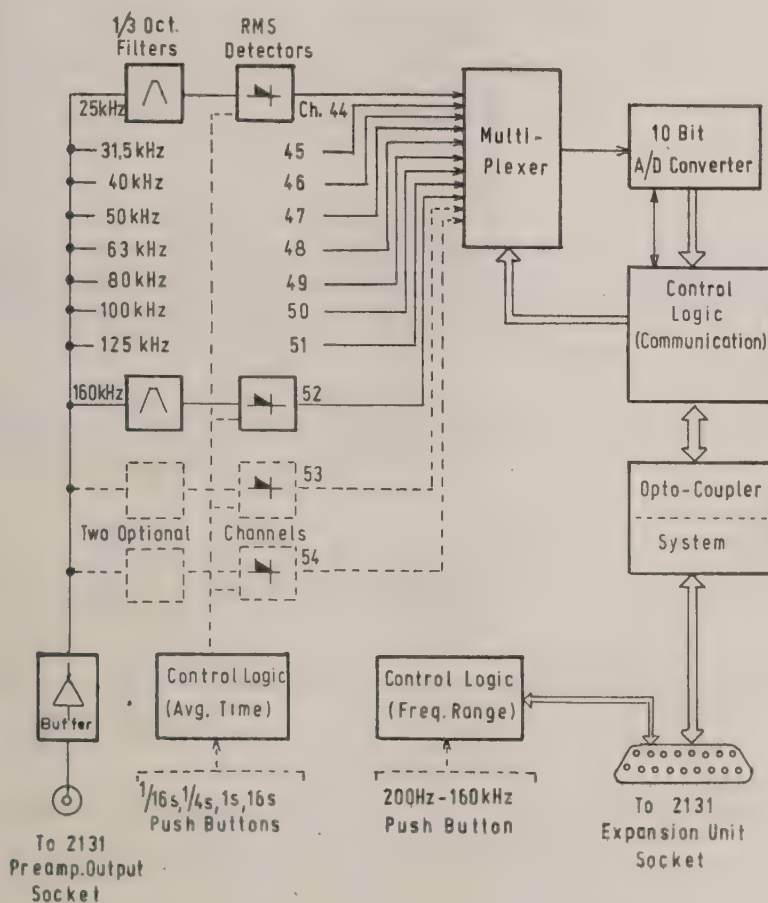


Fig. 2.1

A unity gain amplifier buffers the "Preamp. Output" signal, which is then applied to the filter chain.

Each analog filter has its associated RMS Detector, transforming the filtered level to a DC-LOG equivalent.



On control from 2131 timing signals, the nine (optionally eleven) analog DC levels are multiplexed and converted to digital form via an A/D Converter.

A conversion result (10 bit binary word, representing the level of one of the channels, is returned to the Analyzer on a pulse train basis, before conversion of the next channel.

All signals necessary for the mutual communication between 2131 and the control logic of 5765 are transferred via an opto-coupler system to avoid ground loops.

Note: Analog GND (at "Preamp. Output") and Digital GND (at multi-pin socket) of the 2131 are galvanic connected, and a loop would consequently arise if these were connected to a common reference in 5765.

Circuits located between the coupler system and the multi-pin socket of 5765 are powered from 2131, while the remaining circuitry takes power from the regulated supplies built-in ($\pm 15V$, $+ 5V$).

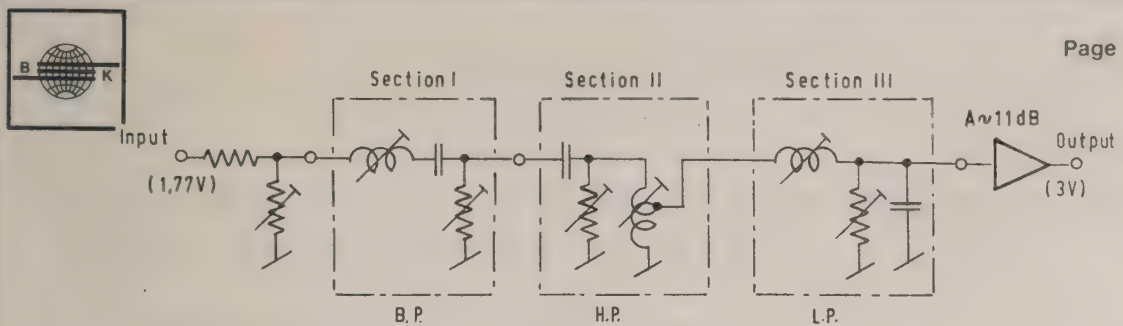
The following text will give a more detailed description of some of the blocks of Fig. 2.1.

1/3 Oct. Filters: (WI 0941 to WI 0949)

The nine 1/3 oct. filters with centre frequencies from 25 kHz to 160 kHz are of similar design.

Each filter may be divided in 3 cascaded subsections (as shown in Fig. 2.2) making up a 6 pole bandpass filter.

Although active components are included in the filter configuration, the filter is basically passive, as the response curves for the individual sections of Fig. 2.2 are achieved through passive components.



○: Signal buffered
(): Full Scale Levels

Fig. 2.2

The resonant frequency of the B.P. section (I) equals the center frequency of the filter (f_0), while the peaking frequencies for the H.P. (II) and L.P. (III) sections are displaced symmetrically around f_0 . The Q-values of the latter sections must be matched and in special relation to the Q-value of the B.P. section to achieve the required bandwidth and a flat filter top.

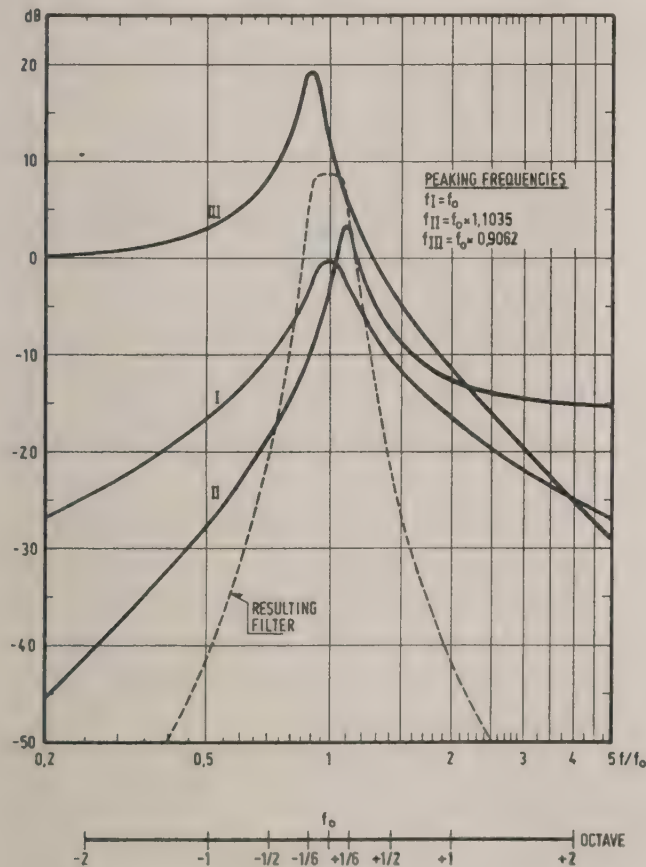


Fig. 2.3 shows the response curve for each of the sections of Fig.2.2 (linear input signal).

The stipulated curve shows the resulting response at the output of section III, when the sections are cascaded, and a linear input signal applied to section I.

This curve, in fact, is the required filter, as the remaining circuitry of the filter board only serves conditioning aims.

Fig. 2.3

The filters are designed to have an Effective Bandwidth of 1/3 octave. On this basis, the shape of a filter is such that the flanks of adjacent filters cross at an attenuation of approx. 3,7 dB from the nominal transmission level.



The true RMS values of the filtered signal levels are detected by precision logarithmic detectors, one for each 5765 channel.

Fig. 2.4 shows the block diagram for the detector.

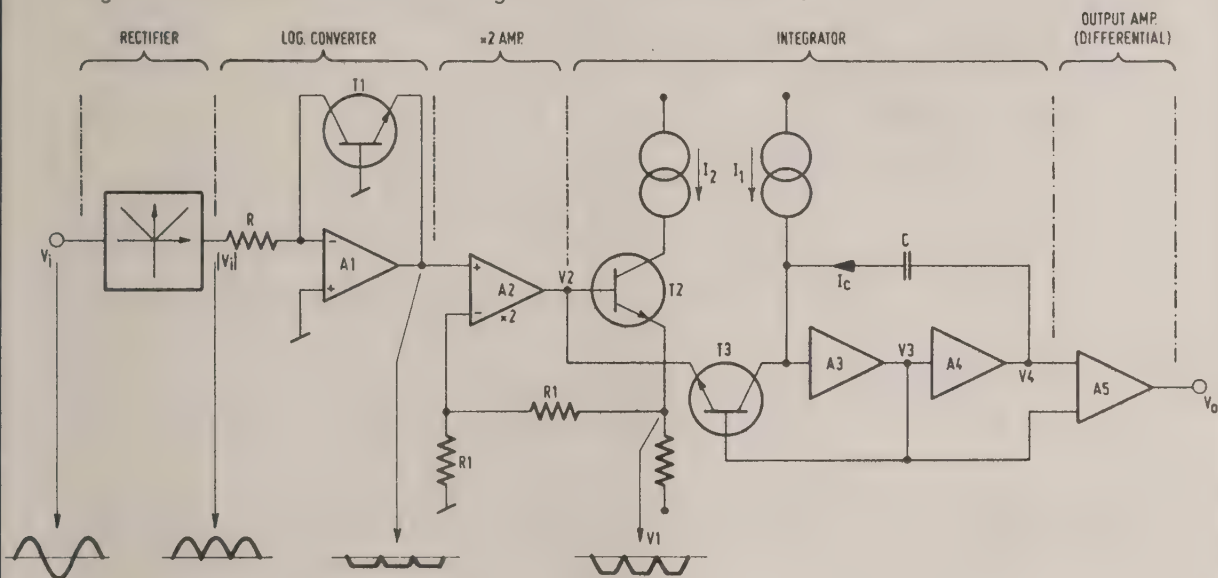


Fig. 2.4

The linear input signal is double rectified and a proportional current ($|V_i|/R$) fed through the log. Element, T1.

Note: The relation: $V_{BE} \approx V_t \ln \frac{I_c}{I_s}$ $V_{CB} \sim 0V$ - for the transistors shown, is essential for the operation of the circuit. Here I_c is the collector current, while I_s and V_t are temperature dependent constants.

$$V_t = \frac{K T}{q}, \text{ where } \begin{cases} K = \text{Boltzman's constant} \\ T = \text{Absolute temperature [} ^\circ\text{Kelvin }] \\ q = \text{Electron charge} \end{cases}$$

$$(V_t \sim 25,7 \text{ mV at } 25^\circ\text{C} ; T = 298^\circ\text{K})$$

The resulting logarithmic output signal from A1 is multiplied by 2, giving:

$$(1) V_1 = - 2 V_t \ln \frac{|V_i|}{R \cdot I_s} = - V_t \ln \frac{V_i^2}{R^2 \cdot I_s^2}$$



The transistors T2 and T3 will cancel the I_s^2 term originating from T1 (eq. 1), and the constant currents I_1 and I_2 are entered instead in the expression for V_3 as stated:

$$(2) \quad V_3 = -V_t \ln \frac{V_i^2}{(I_C + I_1) I_2 R^2}$$

$$\text{Here, } I_C = C \frac{dV_C}{dt} = C \frac{d(V_4 - V_3)}{dt} = (A_4 - 1) C \frac{dV_3}{dt}, \text{ where } A_4 = \frac{V_{i4}}{V_3}$$

By inserting the expression for I_C in (2), the solution to the resulting differential equation can be found to be:

$$(3) \quad V_3 = -2V_t \ln \frac{V_i \text{ (RMS)}}{R \sqrt{I_1 I_2}}$$

$$\text{Here, } V_i \text{ (RMS)} = \sqrt{\frac{1}{\tau} \int_{t-\tau}^t V_i^2 dt}; \quad \tau = \frac{(1 - A_4) C}{I_1} V_t$$

This equation shows that the voltage V_3 is proportional to the logarithm of the RMS value of the input voltage.

The temperature dependency of the voltage V_3 (the V_t -term) is compensated for by letting the amplification $A_4 (=V_{i4}/V_3)$ be inversely proportional to the absolute temp. T , and selected such that the difference voltage $V_{diff.} = V_4 - V_3$ will be independent of temperature.

Selecting $A_4 = -(\frac{A_0 T_0}{T} - 1)$, which in practice is realized with a NTC resistor in combination with fixed resistors, the difference voltage ($V_4 - V_3$) is found to be:

$$(4) \quad V_{diff.} = A_0 \cdot \frac{2 K T_0}{q} \ln \frac{V_i \text{ (RMS)}}{R \sqrt{I_1 I_2}}, \text{ where the "0" index refers to values at selected reference temperature.}$$

Thus: $T_0 = 298^\circ\text{K}$ for $t_0 = 25^\circ\text{C}$

$$A_0 = |A_{40}| + 1 \quad (A_4 \text{ inverting})$$

The difference voltage is seen to be independent of temperature This will also be true for the detection time constant, which (when inserting the expression for A_4) becomes:

$$(5) \quad \tau = \frac{A_0 \cdot C}{I_1} \cdot \frac{K T_0}{q}$$



The output from the RMS detector is made single ended through the differential amplifier A5, the gain of which will affect the final detector sensitivity.

Note: An Off-Set arrangement attached to V_4 will allow adjustment of polarity reversal of the output voltage to a required value within the dynamic input range.

Consequently a constant should be added to the expression for V_{diff} . (4).

The output voltage from the differential amplifier thus becomes:

$$(6) \quad V_0 = K_0 \cdot \ln \frac{V_i \text{ (RMS)}}{R \sqrt{I_1 \cdot I_2}} + V, \text{ where all terms except for } V_i \text{ (RMS) are fixed constants.}$$

$$\text{Note: } K_0 = 2V_{t_0} \cdot A_5 \cdot (|A_{4_0}| + 1), \text{ where } V_{t_0} = \frac{KT_0}{q}$$

Simple calculations will show that a change of +1 dB in the V_i (RMS) level will give occasion for a change in the output level of:

$$A_5 \cdot (|A_{4_0}| + 1) \cdot V_{t_0} \cdot \frac{\ln 10}{10} \text{ Volts.}$$

Thus, for a ref. temp. of 25°C, the detector sensitivity is calculated from:

$$(7) \quad F_D = A_5 \cdot (|A_{4_{25}}| + 1) \cdot 5,9 \text{ mV/dB, and this sensitivity is retained for different temperatures if the variation of } A_4 \text{ ideally cancels the variation of } V_t \text{ with temperature, as was the aim.}$$

Assumptions made on the way to the expression for the output voltage (6) were, that the temp. dependent constants I_s and V_t have identical values for the three transistors of the block diagram. In order for this to be true, the transistors must be closely matched in parameters and in operating temperature.

This is achieved by using transistors of the same type, mounted on a common ceramic substrate together with the NTC resistor (thick film based), which compensates for the final temp. dependency of V_3 (eq. 3).



The detectors of the Expansion Unit are conditioned to have a sensitivity of 48.8 mV/dB, suitable for the further processing of level data via the subsequent A/D-Converter.

Relations between in and output levels are listed below:

V_i RMS [V_{AC}]	V_o [V_{DC}]	dB re. FSD
3,0	2,928	0
0,3	1,952	- 20
0,03	0,976	- 40
0,003	0	- 60
↓	phase reversal	—

The Averaging Time is selectable in four steps (1/16s, 1/4s, 1s and 16s) by switching value of integrating capacitor (C of Fig. 2.4).



Multiplexer & Digital Control Circuits (WI 0954, WI 0955)

The detected DC equivalents to the signal levels in the nine (optionally eleven) new channels are fed to the multiplexer, situated on the "Dig. Contr. II" board (WI 0955).

Here the multiplexed signal is applied to an A/D-Converter which, under control from timing signals, successively converts the analog input levels to 10 bit binary words.

Since the RMS detector has a logarithmic characteristic, the DC-voltage fed to A/D Converter is directly proportional to the dB value for the channel considered.

Note: The least significant bit (LSB) of the A/D Converter equals 4,88 mV and as the RMS detector has been adjusted to have a sensitivity of 48,8 mV/dB, a change of one LSB will correspond to a CRT level change of 0,1 dB.

Thus, when calibrated, the decimal equivalent to the 10 bit binary word resulting from each conversion (bit weight 2^0 to 2^9) will directly equal the dB value for the channel (with the last digit in the decimal number indicating the decimal fraction - 0,1 dB resolution).

Note: Actually the 10 bit words are in CSB (Complementary Straight Binary) code and each bit should hence be thought of as inverted, before finding the decimal equivalent.

Level information for a 5765 channel, however, is transferred to the 2131 Analyzer on a pulse train basis, rather than in the form of a 10 bit data word.

The pulse train is achieved by loading the result from an A/D conversion into a Presetable Binary Counter system, and gating out the number of clock pulses necessary to set the "Carry Output" of the last counter in the chain.



A pulse train consisting of 394 pulses will thus give occasion for 39,4 dB column deflection above the bottom line on the CRT.

Note: Actual level indication will add correction figures for Attenuator position and "Ref. Adj.".

The pulse trains informing about defected levels in the filtered 5765 channels are returned to the Analyzer as the "ACULE" signal.

This signal, of course, must be attended by communication signals (Data Ready, Data Received) to indicate the end of a pulse transfer and that data have been accepted.

The digital circuitry in 5765 for communication with 2131, selection of Mux. channel, control of A/D-converter, Counters, etc. is situated on the WI 0954 and WI 0955 boards.

The timing chart of Fig. 2.5 is illustrative in support of the following description of mode of operation.

Note: The Wiring Diagram lists a key for the mnemonic used for signals.

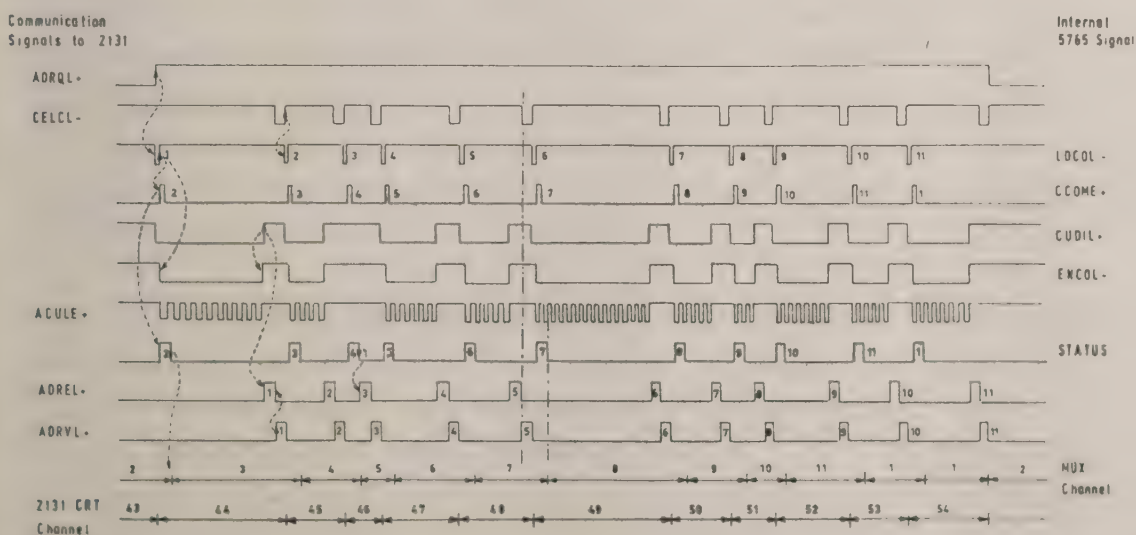


Fig. 2.5



In each "Display Cycle" of the 2131 (repetition rate $\sim 22\text{ms}$) a transfer of data from 5765 is initiated, when the request signal for analog data (ADRQL) goes high after ch. 43 (20 kHz channel).

Note: The Analyzer is designed to accommodate data for up to 11 analog channels. The timing chart covers this case, although the 5765 contains only 9 channels in its standard version (optionally 11, however, by moving jumpers on the WI 0955 board).

At the end of the request signal (but before it returns to low level) the "MUX" will be locked to ch. 1 (25 kHz), while preset to ch. 2 (31,5 kHz) during the processing of the digital channels (low request signal). Thus, when the request signal goes high, the detected level for ch. 2 has settled at the input of the A/D- Converter, while the output of the converter contains the 10 bit conversion result from ch. 1. The latter is loaded into the counter system and on the rear flank of the load impulse a Convert Command for ch. 2 is generated.

When conversion is completed (indicated by STATUS signal - high level $\Rightarrow$ busy) the multiplexer is stepped to ch. 3, which may now settle while data for ch. 1 are transferred on the ACULE signal.

The ACULE signal (1,22 MHz clock pulses) is blocked when the counter system overflows (indicated by the CUDIL signal), whereafter the Data Ready flip-flop is set.

When data have been stored in 2131, a Data Received impulse is returned to 5765, which resets the Data Ready signal.

The counters in 2131 for registering the number of pulses in a pulse train are cleared by the CELCL signal and the trailing edge of this clearing signal will consequently indicate when the 2131 counters are ready to receive new data. This signal, therefore, is used in 5765 to trigger one shuts for generating load and convert commands, now for ch. 2 and ch. 3 respectively.

The ACULE signal will then transfer data for ch. 2 while the MUX. shifts to ch. 4.



Operation proceeds in this way until data for all of the eleven analog channels have been stored in the Display Memory of the Analyzer. As previously stated, this will be updated with new data sets every 22nd ms.

In the standard version of the Expansion Unit the two jumpers on WI 0955 are mounted in positions giving a nine (and not eleven) channel expansion. In this case the MUX. is stepped from ch. 9 to ch. 1, where it is locked until the request signal selects ch. 2 by going low. the two last columns on the CRT are disabled from display by the CUD9L signal (not shown in the Timing Chart).

The Timing Chart of Fig. 2.5 is not drawn to a correct scale, as this would reduce clearness of operation.

Approximate pulse lengths of the different signals, however, are stated here:

LDCOL	} ~ 1 μ s	CELCL	} ~ 20 μ s	STATUS: max. 25 μ s.
CCOME		ADREL		
		ADRVL		

ADRQL: dependent on data sets to be transferred via the ACULE signal (1,22 MHz clock).

The numbers affixed to signals of Fig. 2.5 refer to 5765 MUX channels.

Thus, considering the signals between the two vertical dashed lines on the chart (covering a time history of less than 50 μ s), the following relations exist in sequence.

1. The Analyzer sends Data Received for ch. 5.
2. Conversion result for ch. 6 is loaded into the 5765 Counters, which are then enabled for counting.
3. The settled DC level for ch. 7 is A/D-converted.
4. After conversion the MUX selects ch. 8.



The Timing chart also covers the case of underrange in a 5765 channel (shown for ch. 3). The bits of the binary word loaded into the counter system would then all be ones (obs! CBS word), and the counters hence blocked from counting. The STATUS signal is then used as enable signal for the Data Ready F.F., as the CUDIL signal remained high after loading. As can also be seen from the chart, the underrange of ch. 3 will result in minimum settling time (approx. 40 μ s) for the DC level of ch. 5.

Two settings of the 2131 Analyzer will disable the 5765 channels from display, namely -

- when enabling the "A Weighting" button, or
- by selecting Filter B.W. "1/1 Oct. ".

Both of these settings would lead to incoherency between the spectra parts for digital and analog channels.

Note: The analog channels are disabled by locking the ACULE signal to its high state (disable signals "OCTVL" or "AWGTL" - WI 0954).

AVG. Time & Freq. Range Control Circuits: (WI 0957, WI 0958)

These circuits are both mounted on distance pieces behind the front panel. The control signals for selection of Avg. Time are achieved from a chain of SR-Latches (one for each of the four push buttons). The signal (t_1 to t_4) associated the button last depressed is set low, while the rest are high level.

An "One Shut" arrangement is attached to the circuit. This fires only when power is switched on, and selects then the "1 sec." avg. time (t_3 -signal).

Note: The signals t_2 , t_3 and t_4 are shifted in level and phase on the WI 0954 board before they are applied to the RMS detector chain for avg. control.

(t_1 -signal not used).



The Analyzer is set in its high frequency range by pushing the "Freq. Range" button, whereby the GFRUL signal is momentarily grounded. To indicate that the command has been executed, the Analyzer returns a low level on the FRQUL signal, which turns on the LED of the 5765 control button.

Note: As the Freq. Range circuit (WI 0958) is powered from 2131, this LED might be alight even when the power switch of the Expansion Unit is in its "off" position.

To prevent this confusing condition a relay on the board will disable the LED from lighting, when the 5765 is unpowered.



3. Operation

Initial Set-up Instructions:

1. Before connecting the 5765 to the mains power supply, check that LINE VOLTAGE SELECTOR is correctly set. Adjustment is made by removing the central fuse and withdrawing the voltage selector, which is then repositioned such that the correct line voltage is shown through the slot in its rim.
2. Position the Expansion Unit on top of the 2131 Analyzer and establish the two cable connections:

Multi-cable	-	to 2131 "Expansion Unit" socket
Coax cable	-	to 2131 "Preamp. Output" socket.

Note: Both instruments should be unpowered when connections are made.

Operation Description:

When the Expansion Unit is powered, one of the LEDs of the "Averaging Time" selectors will always be alight.

Note: The "1 sec." avg. time is automatically selected at the instant of switching on the power.

The new channels are continuously updated in accordance with the conditioned "Preamp. Output" signal from the Analyzer.

The level information in them, however, is read back to the Analyzer only if -

- a) the 2131 is in 1/3 Oct. Mode of Operation
- b) the "A Weighting" button on the Front Panel is disabled.



The necessity for analog filtering and RMS detection in the Expansion Unit means, that the following 2131 control features are not active for the new channels:

Lin. Averaging: The analog channels will not participate in the lin. averaging process, but will be continuously updated.

Averaging Time: 4 different Avg. Times for the channels contained in the expansion unit may be selected from the front panel of the 5765. (1/16s, 1/4s, 1s, 16s).

The nine new channels are enabled for display on the 2131 CRT by pressing the "Freq. Range" (200 Hz - 160 kHz) button on the 5765. They are then entered to the right of the 20 kHz standard channel (channel positions 44 to 52).

Note: In case of an eleven channel extension, the two optional 5765 channels will be shown in channel positions 53 and 54 and hence displayed for either selected frequency range.

Partly referring to the description above, the following operating instructions are set out.

Operating Instructions:

1. On 2131 select Filter Bandwidth "1/3 Oct." and disable the "A Weighting" button.
2. Select required Averaging Time.

Note: Preferably the avg. time selected on 2131 should be the same as that selected on its expansion unit to maintain the best coherency between the part spectra for digital and analog channels (especially desirable in case of a non steady input signal).





3. Select Frequency Range for display on the CRT:

1,6 Hz - 1,25 kHz	selectable from 2131
25 Hz - 20 kHz	
200 Hz - 160 kHz	selectable from 5765

Note: Irrespective of selected display range, Center Freq./Level information is available for all channels in the windows above the top line on the CRT, by stepping the 2131 Channel Selector to the required filter.

4. On the 2131 operate the "Input Att.", the "Input Spectrum and Memory Functions", the "Output Spectrum Selectors", e.t.c., as required.

Output from 2131

The first channel output to a Level or XY-Recorder depends on selected display range, while a digital output will cover the complete 1/3 Oct. spectrum, irrespective of frequency range selected for display (see below).

CRT Display Range	Analog Output	Digital Output
1,6 Hz - 1,25 kHz	1,6 Hz - 20 kHz + op.2	1,6Hz -160kHz + op.2
25 Hz - 20 kHz	25 Hz - 20 kHz + op.2	
200 Hz - 160 kHz	200 Hz - 160 kHz + op.2	

Note: The two optional channels of the 5765 are noted as "op.2" in the table.

When not built in, the bottom line reference is output in these two channels.

If the Analyzer is set to 1/1 Oct. mode of operation a digital output will be unchanged from that of a standard 2131.



4. Adjustment Procedure

A: Digital Control Circuits:

The only trimmers are P1 and P2 situated on the WI 0955 board. They adjust OFFSET and GAIN of the A/D Converter respectively, and should not be touched unless absolutely certain that a readjustment is necessary (e.g. after a replacement of the A/D Converter).

For their adjustment the wire jumper J1 (see Circ. Diagram. WI 0955) must be broken and a stable DC voltage applied to the input of the buffer amplifier in front of the A/D Converter.

Note: A "GDN" test pin on the board is used as the reference for the external DC supply.

Procedure:

1. Apply $2,44 \text{ mV}_{\text{DC}}$ and adjust the OFFSET potentiometer (P1) until the 10 - bit binary output word is at the limit to all bits ON. Only LSB unstable.
2. Apply $4,9928 \text{ V}_{\text{DC}}$ and adjust the GAIN potentiometer (P2) until the binary output word is at the limit to all bits OFF. Only LSB unstable.

Note: The inp. voltages stated should be set using a DC-FLUKE.

The state of the individual bits in the output word may be determined with an oscilloscope, successively sensing the data inputs to the counter chain (V 10, 11, 12 - see Circ. Diagram.).

LSB is sensed at V 10 pin 3.

B: 1/3 Oct. Filters:

The adjustment procedure for the 5765 filters presupposes availability of a low impedance signal source (source imp. $< 5\Omega$) with output swing symmetric to common.



Instrumentation must also include facilities for accurate frequency and level read offs.

The table below states characteristic frequencies for each of the three filter sections, which when combined make up the resulting 1/3 Oct. Filter.

Section I			Section II			Section III		
Center Freq.	3dB Frequencies		Center Freq.	3dB Frequencies		Center Freq.	3dB Frequencies	
f_{pI}	f_{uI}	f_{lI}	f_{pII}	f_{uII}	f_{lII}	f_{pIII}	f_{uIII}	f_{lIII}
25,12	28,03	22,51	27,72	29,37	26,31	22,76	23,98	21,47
31,62	35,29	28,34	34,90	36,98	33,13	28,66	30,19	27,04
39,81	44,43	35,67	43,93	46,56	41,70	36,08	38,01	34,04
50,12	55,93	44,91	55,31	58,61	52,50	45,42	47,85	42,85
63,10	70,41	56,54	69,63	73,79	66,09	57,12	60,24	53,95
79,43	88,65	71,18	87,65	92,90	83,21	71,98	75,84	67,92
100,0	111,6	89,61	110,4	117,0	104,8	90,62	95,48	85,50
125,9	140,5	112,8	138,9	147,2	131,9	114,1	120,2	107,6
158,5	176,9	142,0	174,9	185,4	166,0	143,6	151,3	135,5

Notice that the 3 dB frequencies for section I are symmetric to the center frequency of the filter (B.P. section) while nonsymmetric to the peaking frequency in the sections II and III (H.P. & L.P. sections respectively).

An extension board must be used to gain access to the filter trimmers.

Procedure:

Section III:

Unsolder capacitor C2 at the point marked "B" (See Circuit Diagram) and apply an input signal (source imp. $< 5\Omega$) to point "A" (common connection between C2, R2, L2).

Set the input voltage to 200 mV and the frequency to f_{pIII} . Connect a Measuring Amplifier to tp.3 and adjust L3 for max. output voltage, which should be approx. +3 dB rel. input level. If not, adjust P3.



Adjust input level for a suitable needle deflection at $f_{p_{III}}$ and observe meter indications at the 3 dB frequencies from table.

Attenuation should be the same (if not, fine adjust L3) and 3 dB (if not, fine adjust P3).

Section II

Apply the input signal (200 mV, $f = f_{p_{II}}$) to the free end of C2 (point "B"), and connect the Measuring Amplifier to tp.2.

Adjust L2 for max. output voltage, which should be approx. +3 dB rel. input level. If not, adjust P2.

Adjust input level for a suitable needle deflection at $f_{p_{II}}$ and observe meter indications at the 3 dB frequencies from table.

Attenuation should be the same (if not, fine adjust L2) and 3 dB (if not, fine adjust P2).

Sections II - III

With input signal still applied to the free end of C2, observe the response on the Measuring Amplifier connected to tp.3 again, when sweeping around the centre frequency of the filter.

Symmetrical peaks should occur at frequencies $0,925 \times f_0$ and $1,081 \times f_0$.

Peaking levels should exceed the valley level at f_0 by approx. 1,25 dB.

Note: Probably the trimmers in section III (L3,P3) will need an extra adjustment to achieve the best accordance with the statements above.

Section I

Remount C2 and apply the input signal (2V, $f = f_0$) to filter input.

Connect the Measuring Amplifier to tp.1 and adjust L1 for max. output voltage.



Adjust input level for a suitable needle deflection at f_0 and observe meter indications at the 3 dB frequencies from table, Attenuation should be the same (if not, fine adjust L1) and 3 dB (if not, adjust P1).

Total Filter:

Connect the Measuring Amplifier to filter output and apply 1,77 V RMS (Sine) to Filter Input at $f = f_0$.

Adjust P4 for 3 V RMS output level.

Vary the frequency around the center frequency.

Response should be within $\pm 0,5$ dB rel. f_0 level for frequencies within $\pm 1/12$ Oct. from f_0 .

At the frequencies " $f_0 + 1/6$ Oct." and " $f_0 - 1/6$ Oct." the filter flanks should be down 3.7 dB ± 1 dB.

The checking frequencies stated can be read off from the table shown.

In case the filter needs a fine adjustment, thoroughly observe the shape of the filter top to deduce which trimmers are most effectively adjusted to achieve the required effect.

- 1/6 Oct.	- 1/12 Oct.	Center Freq. (kHz)	+ 1/12 Oct.	+ 1/6 Oct.
22,39	23,71	25,12	26,60	28,18
28,18	29,85	31,62	33,49	35,45
35,45	37,58	39,81	42,16	44,66
44,66	47,31	50,12	53,08	56,21
56,21	59,56	63,10	66,83	70,77
70,77	74,98	79,43	84,13	89,09
89,09	94,40	100,0	105,9	112,3
112,3	118,8	125,9	133,3	141,3
141,3	149,6	158,5	167,8	177,8

C: RMS Detectors:

The nine RMS Detectors (WI 0950) are all identical.

In case a readjustment of one of the detectors is found necessary, select the faulty 5765 channel with the 2131 Channel Selector and make adjustments on the basis of level indications in the window on the CRT, when switching the signal level to the 2131 input in accurate steps of 10 dB.

Note: Output level from the signal source should be independent of frequency for frequencies up to 200 kHz.



Adjustments must be carried out with the 2131 Attenuator in a nonsensitive position (e.g. 50 dB bottom ref. level) and after the instruments have warmed up for at least 15 minutes.

One of the low Averaging Times (e.g. 1/4s) should be selected for a quicker identification of the effect of an adjustment.

A complete readjustment will probably not be necessary unless a component in the "ac-part" of the detector has been replaced.

Initially, therefore, proceed as follows:

- a. Change the input signal (freq. = center freq. for the channel to be checked) in steps of 10 dB within the central 40 dB window of the CRT.

Differences between levels read out should correspond to the actual changes in the input levels in dB.

If not, adjust the sensitivity potentiometer, P5.

- b. Adjust the signal source to a level which makes the standard 2131 channels deflect to the line 10 dB below FSD, when exposed at their centre frequency.

Return to the frequency stated in item "a" and adjust P4 until the column for the channel considered deflects to the same line.

- c. Check the channel for linearity over the full CRT range by changing the input level in steps of 10 dB (from top to bottom line), while observing levels read out.

If necessary, readjust P5 for better overall linearity.

Repeat item "b" if P5 is touched.

In case these adjustments prove not to be sufficient for achieving an overall linearity within tolerances, the whole detector must be readjusted at the center frequency "fc" of the 5765 channel concerned, following the procedure listed below.



1. Apply an input signal to the Analyzer which in level is approx. 10 dB higher than the bottom ref. level of the CRT ($f = f_c$)

Note: If the corresponding column deflection for the 5765 channel diverges significantly from the correct value, adjust P4 for better agreement.

Check by means of an oscilloscope connected to the anode of Q10 that the unsmoothed full wave rectified logarithmic signal is symmetrical.

If not, adjust P1.

Note: Oscilloscope is set in AC mode and high sensitivity selected.

2. Change the input level "+ 10 dB" and "- 10 dB" rel. level of item 1 and observe if the differences between levels read out are the same (not necessarily 10 dB, however,).

If not, adjust P2.

3. Repeat items 1 and 2 for best agreement with set outs.
4. Adjust the trimmers P5 and P4 as described in the previous items "a" and "b".
5. Adjust the input level to 14 dB below a FSD.
Increase the input level 20 dB in steps of 10 dB and adjust P3 for best agreement between levels read out, and the actual changes in input level.
6. Check the overall linearity as described in item "C".



5. 2131 Modifications

The following description may be considered also as Instructions for Modification.

ZT 0051 LP Filter / A-Filter

R 45 changed to 6,8 k Ω (original value: 4,7 k Ω)

JZ 0025 Mother Board for ZD 0114 and ZT 0051

New wire (to be connected to the MI-socket) soldered to terminal 21 of the socket for ZT 0051.

Note: The Display Unit must be removed to gain access to the soldering terminal.

JZ 0010 Mother Board for digital Plug-in Circuits

1. Above mentioned wire (from pin 21/ZT 0051) connected to pin 16 of the MI-socket (Flat Cable socket with connection to the "Expansion Unit" socket).

Note: The original connection to MI pin 16 (ACUME+) signal is cut from the bottom side of the Mother Board.

2. New wire (to the Exp. Unit socket) soldered to the test pin marked "+ 5 V Group 3".

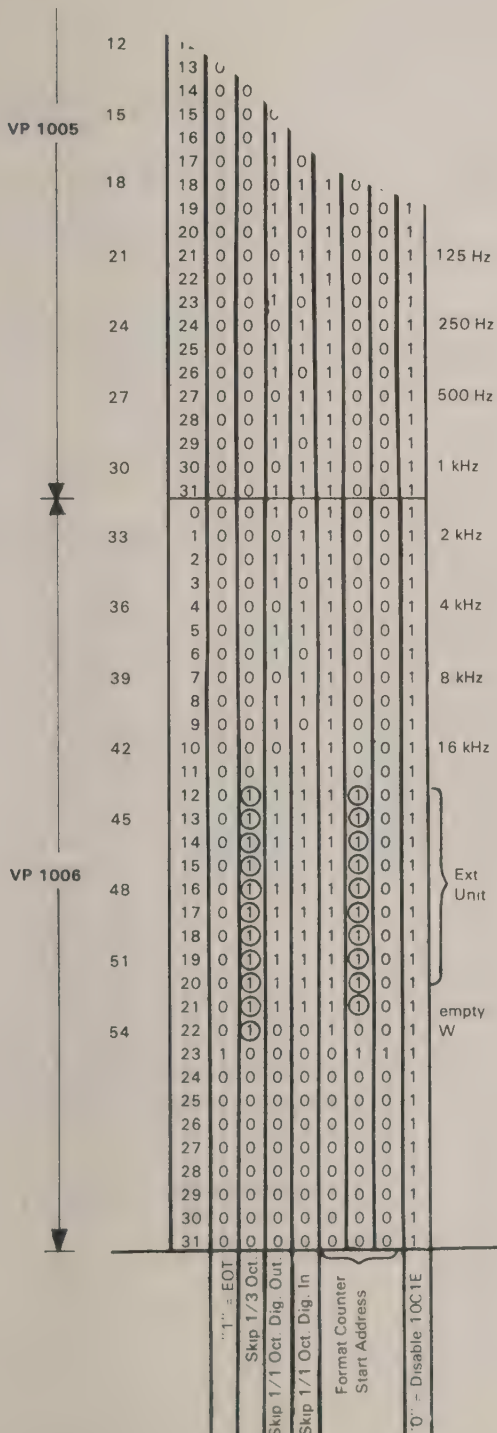
JZ 0009 P.C. Board for Rear Panel Sockets

" + 5 V " wire from JZ 0010 connected to pin 11 of the 15 pole "Expansion Unit" socket.

Note: Original connection to the MI socket (pin 4) of JZ 0009 is cut.

ZD 0098

In order to make possible a digital read in/out of levels in the new channels (Analyzer in 1/3 Oct. Mode) the Read Only Memory VP 1006 is replaced with a reprogrammed Unit WT 0026 (see Fig.5.1).



The WT 0026 is programmed exactly as its predecessor except in the word addresses 12 to 22, where the circled "1"s of the VP 1006 ROM are instead "0"s in the replacement package.

Fig. 5.1

Partial extract from
parts List to ZD 0098.



6. Specifications

Number of Channels:

Nine Third Octave Channels with centre frequencies from 25 kHz to 160 kHz.
Two optional channels available.

Note: Two jumpers (J2 and J3) on the WI 0955 board must then be repositioned as shown in the Component Location Diagram:

n ~ nine	}	channel expansion.
e ~ eleven		

Third Octave Filters:

6 pole Analog Filters.

Filter shape in accordance with IEC 225-1966, DIN 45652 and ANSI S1.11-1966 Class III.

Peak to valley ripple in passband: < 0.5 dB.

The total integrated random white noise power passed by a filter equals that which would be passed by an ideal third octave filter.

RMS Detectors:

Detector Characteristic: Logarithmic true RMS detection.

Dynamic Range : > 60 dB.

Averaging Times : 1/16s, 1/4s, 1s, 16s ± 10%.
Selectable from 5765 push buttons.

Crest Factor Capability: 2.8 (9 dB) at FSD, increasing proportionally to 30 (30 dB) at 21 dB below FSD.

Detection accuracy is not influenced for input signals with crest factors up to 15, while ± 1 dB must be added for higher crest factors.

Overall Accuracy:

The reference signal for calibration of the 5765 channels is a sine wave signal applied to the input of the Analyzer, with the Input Attenuator set to: "50 dB bottom line level" on CRT.



At the centre frequency of a 5765 filter, accuracy* is better than:

± 0.5 dB	0 to 35 dB below FSD	} at 25°C
± 1 dB	35 to 45 dB below FSD	
± 2 dB	45 to 55 dB below FSD	
± 3 dB	55 to 60 dB below FSD	

For other Attenuator settings the tolerances for the Frequency Response of the Preamp. Output signal from the Analyzer must be added:

± 0.2 dB	$f < 100$ kHz
± 0.5 dB	100 kHz to 200 kHz.

For operation at different ambient temperatures, tolerances are increased with:

± 0.03 dB/°C	0 to 50 dB below FSD
± 0.1 dB/°C	50 to 60 dB below FSD

*Tolerances stated are overall (valid from Analyzer Input) and apply to detected levels with at least a 10 dB noise margin.

Note: In sensitive attenuator positions and with shorted input, the residual column deflection indicates the noise level in the channel.

Representation of Channels:

In order for the new channels to maintain coherency to the spectrum present for the 2131 standard channels, level data from 5765 are read back to the Analyzer only if:

- a) 2131 is in 1/3 Oct. Mode of Operation
- b) "A-weighting" button on 2131 is disabled.

The nine high frequency channels are entered immediately after the 20 kHz standard channel of 2131, that is, in channel positions 44 to 52.

In case of an 11 channel expansion, the two optional channels will be shown in channel positions 53 and 54.



Display Ranges:

The new channels are entered for display on the CRT on command from a control button on 5765:

"Freq. Range 200 Hz - 160 kHz" -

which is electrically interlocked with the two "Freq. Range" buttons of the Analyzer.

The complete spectrum is thus divided in three display ranges, covering:

Freq. Range	1.6 Hz - 1.25 kHz	ch. 2-31	+ 53,54
	25 Hz - 20 kHz	ch.14-43	+ 53,54
	200 Hz - 160 kHz	ch.23-52	+ 53,54

Note: When built-in, the two optional channels are displayed for either selected Frequency Range.

Alphanumeric Read-outs:

When selected by Channel Selector, "Center Frequency" and "Level" data for the new channels are entered in the windows above the top line on the CRT. (Irrespective of selected Display Range).

Resolution for level indication: 0.1 dB.

Note: The "Center Frequency" window is extinguished, when one of the two optional channels is selected. If not built-in, the "Level" window will show the CRT bottom line reference level.

Output from 2131:

A Digital output will cover all channels, while an Analog output will comprise only part of the complete spectrum. See Operation Section page 3.3 for details.

Operating Temperature Range:

5°C to 40°C.



Power Requirements:

100, 115, 127, 220, 240 V AC, 50-60 Hz
approx. 38 VA

Dimensions and Weight:

Height: 133 mm (5.25 in)
Width : 430 mm (16.9 in)
Depth : 320 mm (12.6 in)
Weight: 8 kg (17.6 lb)

Accessories Included:

- 1 AN 0010 Mains Cable
- 1 AO 0133 Coaxial cable
- 1 WL 0234 15-core connection cable
- 2 VF 0031 1/4A Fuse
- 2 VF 0023 1/2A Fuse

7. Parts ListPRINTED CIRCUITS:

WX 0853	with components	WI 0914 to 949	1/3 Oct. Filter
WX 0865	" "	WI 0950	RMS Detector
WX 0533	" "	WI 0951	+ 5V Reg.
WX 0532	" "	WI 0952	Rectifier
WX 0887	" "	WI 0953	Inp. Amp.
WX 0880	" "	WI 0954	Dig. Contr. I
WX 0879	" "	WI 0955	Dig. Contr. II
WX 0928	" "	WI 0956	Rectifier
WX 0889	" "	WI 0957	Avg. Time Contr.
WX 0886	" "	WI 0958	Freq. Range Contr.
WX 0885	Motherboard.		

MISCELLANEOUS: (See Wiring Diagram)

Circuit Diagr. Ref.	Component Type	Stock Ref.
C1 to C6	Electrolytic 470 μ F/16V	CE 0337
C7,8	" 1000 μ F/6,3V	CE 0210
F1	Fuse Slow 1/4A; 240,220V	VF 0031
	" " 1/2A; 127,115,100V	VF 0023
N1	Power Switch	NN 0014
O1	Mains Voltage Selector	JS 0001
S1	15-pin Socket	JJ 1504
S2	BNC Socket	JJ 0130
T1	Mains Transformer	
V1	+ 15V Reg.	7815 VE 0096
V2	- 15V Reg.	7915 VE 0097
Z1	Mains Socket with Filter	ZS 0306
	Print Connector (40 pole)	WJ 0047
	Print Connector (18 pole)	WJ 0035

Circuit
Diagr. Ref.Component
TypeStock
Ref.1/3 Oct Filters WI 0914 to WI 0949Components common to all filters:

C4	Polyester	68nF/250V	CS 0406
C5	Ceramic	10pF/400V	CK 1100
C6,7	"	47nF/16V	CK 4471
C8,9	Tantalum	15μF/20V	CF 0010
R4	Carbon	5% 22kΩ	RB 4220
R5	"	" 3,9kΩ	RB 3390
R6,7,9,10	"	" 4,7kΩ	RB 3470
R8	"	" 3,3kΩ	RB 3330
R11	Metal	1% 3,01kΩ	RF 3301
R12	"	" 10,5kΩ	RF 4105
R13	"	" 4,99kΩ	RF 3499
R14	Carbon	5% 10kΩ	RB 4100
R15,16	"	" 10kΩ	RB 1100
P4	Cermet	2kΩ	PG 2212
V1,2,3	Si. NPN	BC 107	VB 1032
V4	Op. Smp.	LM 318	VE 0050

Components dependent on center freq. of filter:

Center freq. kHz	Circuit I						Circuit II						Circuit III					
	L1	C1	R1	P1	L2	C2	R2	P2	L3	C3	R3	P3	L3	C3	R3	P3	L3	C3
	mH	PF	CT	kΩ	mH	nF	CT	kΩ	mH	nF	CT	kΩ	mH	nF	CT	kΩ	mH	nF
25	50 0884	750 1146	1,2 3120	1 2113	11 0879	3,16 1164	12 4120	10 3123	14 0880	3,16 1164	15 4150	10 3123	14 0880	3,16 1164	15 4150	10 3123	14 0880	3,16 1164
31,5	50 0884	470 1111	1,8 3180	1 2113	8,3 0875	2,7 1158	—	—	10 0878	2,7 1158	—	—	10 0878	2,7 1158	—	—	10 0878	2,7 1158
40	50 0884	300 1112	1,8 3180	2 2215	7,1 0874	2,0 1123	—	—	9 0876	2,0 1123	—	—	9 0876	2,0 1123	—	—	9 0876	2,0 1123
50	50 0884	180 1140	2,7 3270	2 2215	5,6 0871	1,6 1103	—	—	7,1 0873	1,6 1103	—	—	7,1 0873	1,6 1103	—	—	7,1 0873	1,6 1103
63	50 0884	110 1136	3,3 3330	5 2516	4,5 0870	1,25 3219	—	—	5,7 0872	1,25 3219	—	—	5,7 0872	1,25 3219	—	—	5,7 0872	1,25 3219
80	14 0880	270 1143	1,2 3120	1 2113	3,6 0868	1,0 1132	—	—	4,5 0869	1,0 1132	—	—	4,5 0869	1,0 1132	—	—	4,5 0869	1,0 1132
100	14 0880	160 1130	1,8 3180	1 2113	2,8 0865	0,82 1121	—	—	3,5 0867	0,82 1121	—	—	3,5 0867	0,82 1121	—	—	3,5 0867	0,82 1121
125	10 0878	150 1139	1,5 3150	1 2113	2,3 0864	0,62 1109	—	—	2,9 0866	0,62 1109	—	—	2,9 0866	0,62 1109	—	—	2,9 0866	0,62 1109
160	10 0878	82 1162	2,2 3280	1 2113	1,8 0862	0,499 1114	—	—	2,3 0863	0,499 1114	—	—	2,3 0863	0,499 1114	—	—	2,3 0863	0,499 1114



Circuit Diagr. Ref.	Component Type		Stock Ref.
LOGARITHMIC RMS DETECTOR (Nine Channels) WI 0950			
C1, 22, 31	Polyester	100nF/250V	CS 0402
C2, 14, 16	Ceramic	150pF/200V	CK 2151
C3, 13, 24	"	10pF/400V	CK 1100
C4, 5	Tantalum	15μF/20V	CF 0010
C6	Ceramic	33pF/400V	CK 1330
C7,8	"	15pF/400V	CK 1150
C9, 11, 15	"	22nF/63V	CK 4220
C12	"	47nF/30V	CK 4470
C17	"	4,7pF/400V	CK 0471
C18, 19	"	47nF/16V	CK 4471
C20	"	18pF/400V	CK 1180
C25	Polyester	39nF/250V	CS 0048
C26	Polycarbonate	120nF/250V	CS 0050
C27	Polyester	560nF/250V	CS 0052
C28	"	10μF/63V	CS 0806
C29	Ceramic	22pF/400V	CK 1220
C30	"	56pF/400V	CK 1471
P1,4	Cermet	47kΩ	PG 3470
P2	"	100kΩ	PG 4107
P3	"	100 Ω	PG 1106
P5	"	4,7kΩ	PG 2471
Q1,6,7,8,9	Si.	1N 4148	75V/100mA
Q10,14,15,16	"	"	"
Q2,3,11,12,13,	Zener	1N 4567	6,4V ref.
Q4,5	Si.	HP-5082-2302	
Q17	Zener		4,0-4,6V/5mA
R1,7,8,16,17	Metal	1%	4,99kΩ
R2	"	"	4,87kΩ
R3,18,23	"	"	100Ω
R4,19	"	"	169kΩ
R5,6	"	"	8,66kΩ
R9,12	"	"	3,32kΩ
R10,11	"	"	110Ω
R13,15	"	"	845Ω
R14	"	"	13,3kΩ
R20,22,50,51	"	"	4,99kΩ
R21	"	"	7,50kΩ
R24,25	"	"	56,2kΩ
R26,53,54	"	"	10,0kΩ
R27	"	"	2,21kΩ
R28	"	"	221Ω

Circuit
Diagr. Ref.Component
TypeStock
Ref.WI 0950 - Continued

R29,30	Metal	1%	1,00k Ω	RF 3100
R31	"	"	46,4 Ω	RF 1464
R32	"	"	12,7k Ω	RF 4127
R33	"	"	14,3k Ω	RF 4143
R34	"	"	7,68k Ω	RF 3768
R35	"	"	2,87k Ω	RF 3287
R36,39	"	"	17,4k Ω	RF 4174
R37	Carbon	2%	22,8M Ω	RH 0015
R38	Metal	1%	15,0k Ω	RF 4150
R40,43	Selected to R41 (R40=R43)			
R41	NTC Resistor (inside V9)			
R42,49,58	Selected to R41			
R45	Metal	1%	3,24k Ω	RF 3324
R46,47,48	Carbon	5%	10M Ω	RB 7100
R52	Metal	1%	7,87k Ω	RF 3787
R55,56	"	"	24,9k Ω	RF 4249
R57	"	"	150 Ω	RF 2150
V1,6,8,17	Op. Amp.		LM 201A	VE 0084
V2,4	Si. PNP		BF 450	
V3,5,7	Si. NPN		BF 240	
V9a,b,c + R41	3 x Si. NPN + NTC resistor			ZE 0256
V10,13	Op. Amp.		356H	
V11,12	Si. PNP		BC 179B	VB 0100
V14,15,16	FET		NF 510	VB 1034
V18	Op. Amp.		LM 301A	VE 0017



Circuit Diagr. Ref.	Component Type		Stock Ref.
<u>5V REGULATOR WI 0951</u>			
C1,2	Polycarbonate	0,1 μ F/100V	CS 0409
V1	Volt. Reg. (5V)	LM 309	VE 0022
<u>RECTIFIER WI 0952</u>			
C1,2	Electrolytic	1000 μ F/50V	CE 0527
Q1,2,3,4	Si. 1N 4004	1A/400V	QV 0237
<u>INPUT AMPLIFIER WI 0953</u>			
C1	Polycarbonate	0,47 μ F/100V	CS 0335
C2,3	Polyester	100nF/250V	CS 0402
Q1,2	Si. BAY 73	225mA/100V	QV 0213
R1	Carbon 5%	100k Ω	RB 5100
R2	" "	10k Ω	RB 4100
V1	Volt. Follower	LM 310	VE 0023
<u>DIGITAL CONTROL I WI 0954</u>			
C1,5	Electrolytic	450 μ F/16V	CE 0337
C2	"	220 μ F/6V	CE 0208
C3	Ceramic	4,7nF/30V	CK 3473
C4	"	2,7nF/40V	CK 3270
C6 to C11	"	47nF/16V	CK 4471
R1,2,3	Carbon 5%	2,2k Ω	RB 3220
R4,5,6	" "	8,2k Ω	RB 3820
R7,8,9	" "	15k Ω	RB 4150
R10,11,12,13,14	" "	2,2k Ω	RB 3220
R15,17	" "	1k Ω	RB 3100
R16,20,21	" "	180 Ω	RB 2180
R18,19,22,25,26	" "	5,6k Ω	RB 3560
R23,24	" "	560 Ω	RB 2560
R27,30	" "	1k Ω	RB 3100
R28,29	" "	320 Ω	RB 2330

Circuit
Diagr. Ref.Component
TypeStock
Ref.WI 0954 - Continued

V1,2,3	Si. PNP	BC 177	VB 0071
V4	2 x 4 Inp. NAND	7420	VD 0007
V5,10	6 x INV. Schm. Tr.	7414	VD 1310
V6	Opto Coupler	5082-4364	
V7,8	" "	5082-4355	
V9	3 x 3 Inp. NOR	7427	VD 0053
V11	6 x INV.	7404	VD 0004
V12	4 x 2 Inp. NAND	7400	VD 0002
V13	2 x J-K Flip-Flop	74LS112	VD 1005

DIGITAL CONTROL II WI 0955

C1,2	Electrolytic	100 μ F/16V	CE 0310
C3	Ceramic	27pF/100V	CK 1271
C4	"	4,7nF/30V	CK 3473
C5,8,9	Tantalum	2,2 μ F/35V	CF 0022
C6,7,11,12	Ceramic	47nF/16V	CK 4471
C10	Electrolytic	470 μ F/16V	CE 0337
P1,2	Cermet multiturn	100k Ω	PG 4110
Q1,2	Si. BAX 16	300mA/150V	QV 0217
R1	Carbon 5%	100 Ω	RB 2100
R2	" "	1k Ω	RB 3100
R3	" "	3,9k Ω	RB 3390
R4,5	" "	270k Ω	RB 5270
R6	" "	3,9M Ω	RB 6390
R7	" "	220 Ω	RB 2220
R8	" "	2,2k Ω	RB 3220
R9	" "	560 Ω	RB 2560
R10,11,13,14	" "	1k Ω	RB 3100
R12	" "	10k Ω	RB 4100
V1	8 ch. Analog MUX	AM 3705CD	
V2,3	2 " " "	HI 200	VE 0070
V4,10,11,12	Synchr. 4-Bit Counter	74LS161	VD 1043
V5	3 x 3 Inp. NAND	74LS10	VD 1049
V6,9	2 x D type Flip-Flop	74LS74	VD 1001
V7	6 x INV.	7404	VD 0004
V8	2 x J-K Flip-Flop	74LS112	VD 1005
V13	Op. Amp.	LM301	VE 0017
V14	10 Bit A/D CONV.	ADC80AG-10	
X1	4,88MHz Crystal		MB 0012

Circuit
Diagr. Ref.Component
TypeStock
Ref.RECTIFIER WI 0956

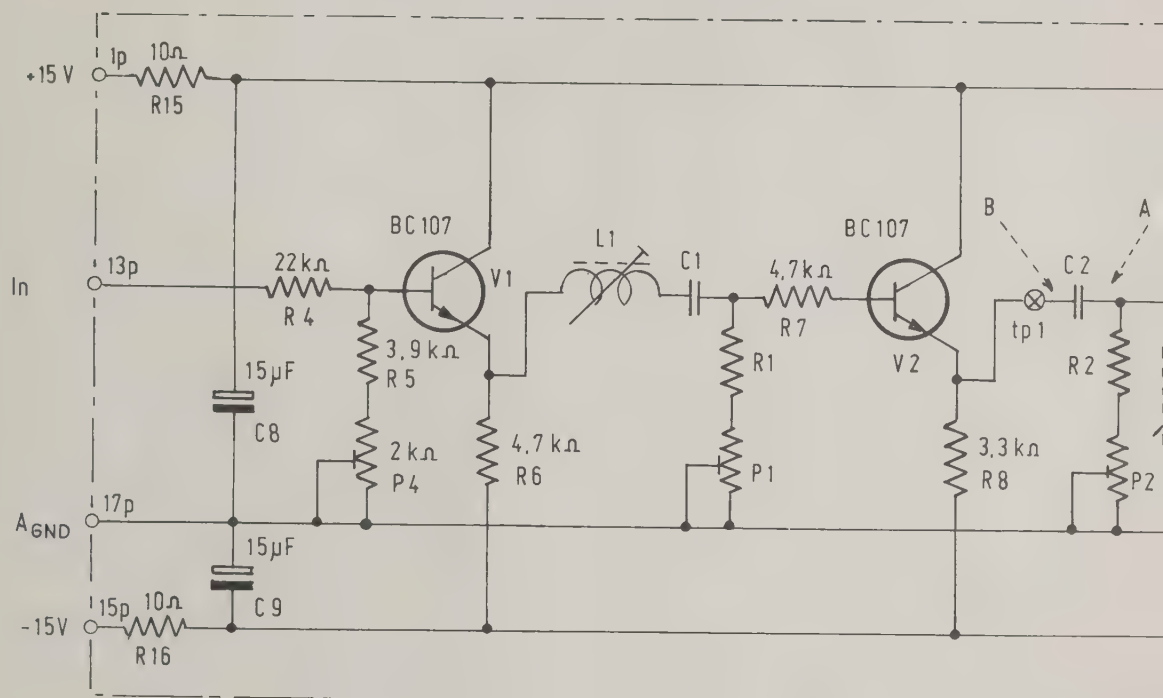
C1,2	Electrolytic	2,2mF/40V	CE 0452
C3,4	Polycarbonate	0,33μF/100V	CS 0350
Q1,2,3,4	Si. 1N4004	1A/400V	QV 0237

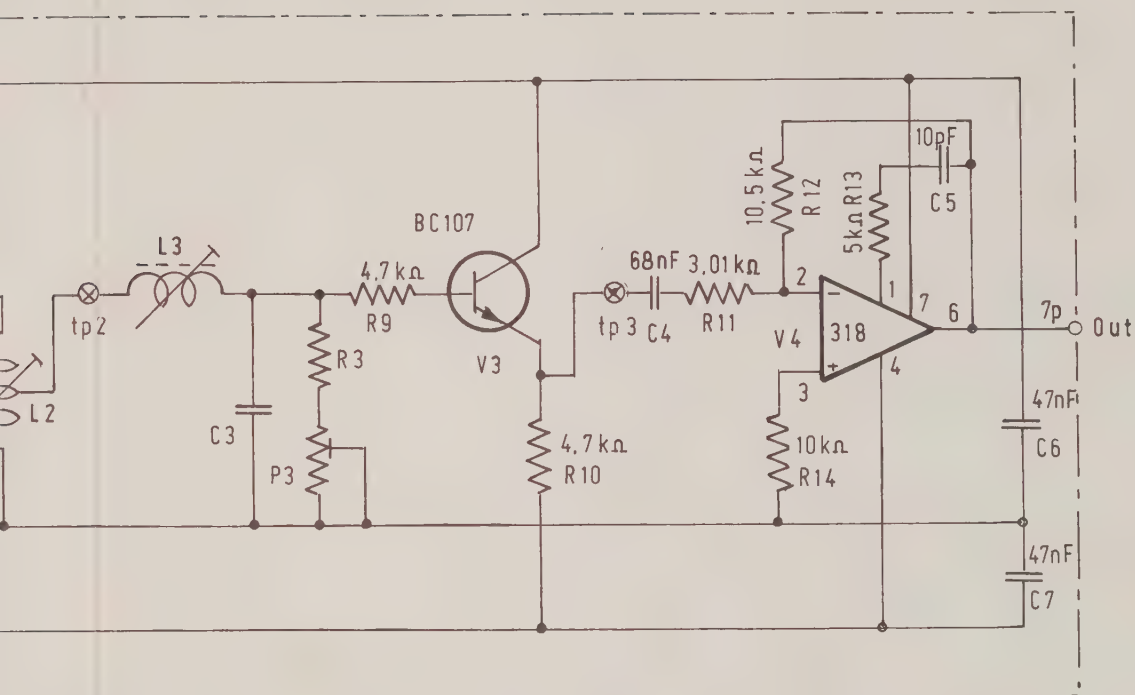
AVERAGING TIME CONTROL WI 0957

C1,2,3,4	Ceramic	4,7nF/30V	CK 3473
C5,6	Tantalum	10μF/16V	CF 0059
C7,8	Ceramic	47nF/12V	CK 4471
C9	Electrolytic	100μF/16V	CE 0310
N1,2,3,4	Push button with LED		NT 0042
R1,2,3,4,7	Carbon 5%	5,6kΩ	RB 3560
R5	" "	390Ω	RB 2390
R6	" "	2,7kΩ	RB 3270
R8	" "	2,2kΩ	RB 3220
R9	" "	100kΩ	RB 5100
R10	" "	10kΩ	RB 4100
R11	" "	22kΩ	RB 4220
R12	" "	1kΩ	RB 3100
V1	4 x SR Latches	74279	VD 0073
V2	4 x 2 Inp. NAND	7400	VD 0002
V3	2 x 4 Inp. NAND	7420	VD 0007
V4	Timer	555	VD 0062
V5	Silicon NPN	BC 107	VB 0032

FREQUENCY RANGE CONTROL WI 0958

C1	Electrolytic	22μF/25V	CE 2002
N1	Push button with LED		NT 0042
O1	Relay		OC 0072
R1	Carbon 5%	8,2kΩ	RB 3820
R2	" "	2,2kΩ	RB 3220
R3	" "	390Ω	RB 2390
V1	Silicon PNP	BC177	VB 0071



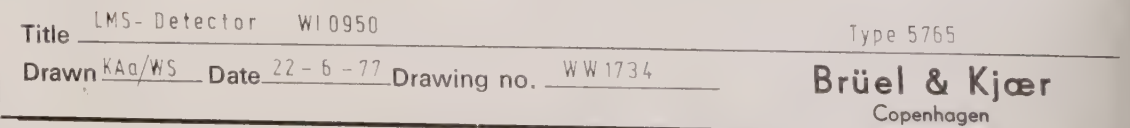


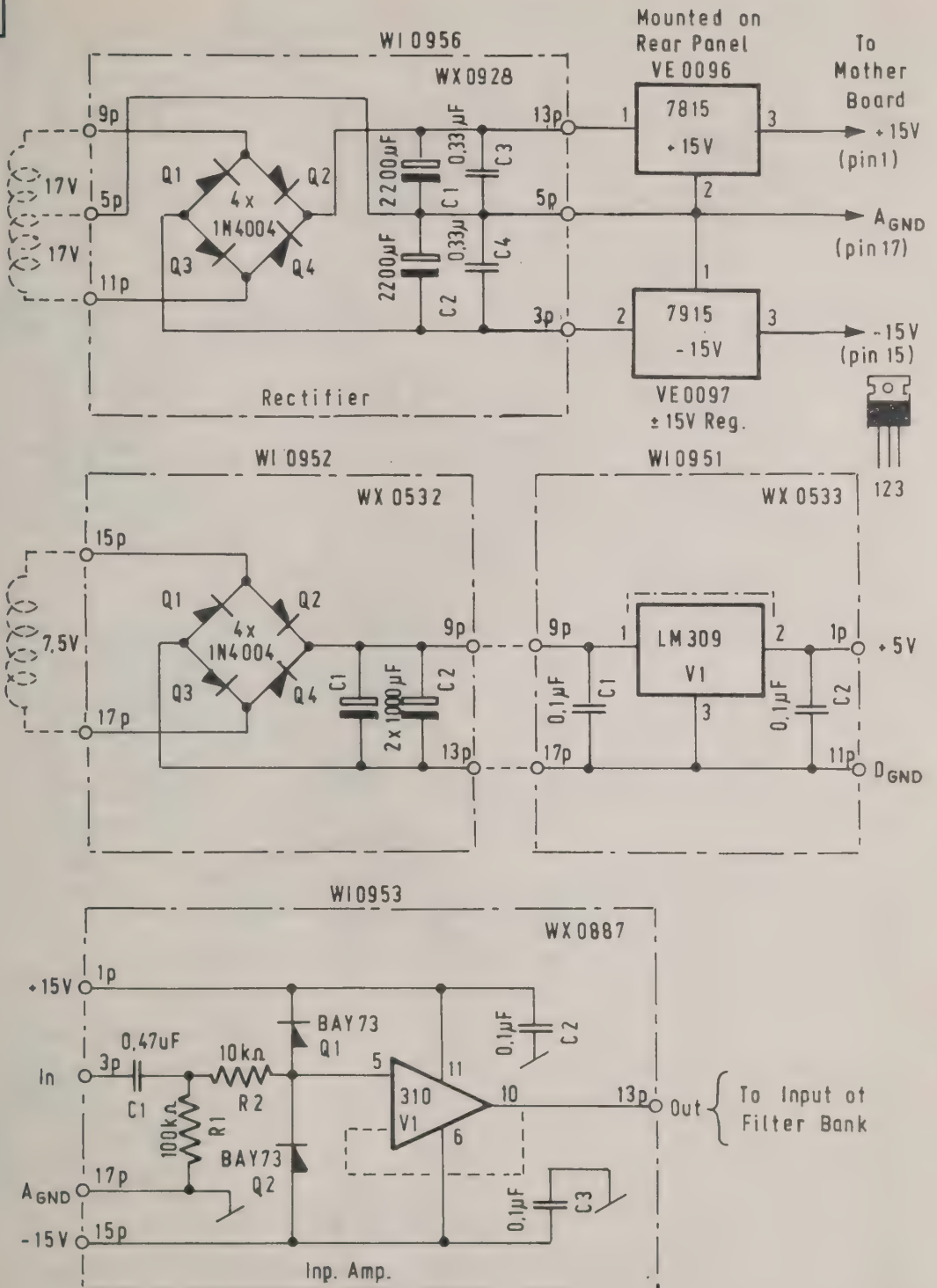
Title 1/3 Oct. Filters (25kHz to 160kHz) W1 0941 to W1 0949

Type 5765

Drawn FLH/WS Date 21-6-77 Drawing no. WW 1730

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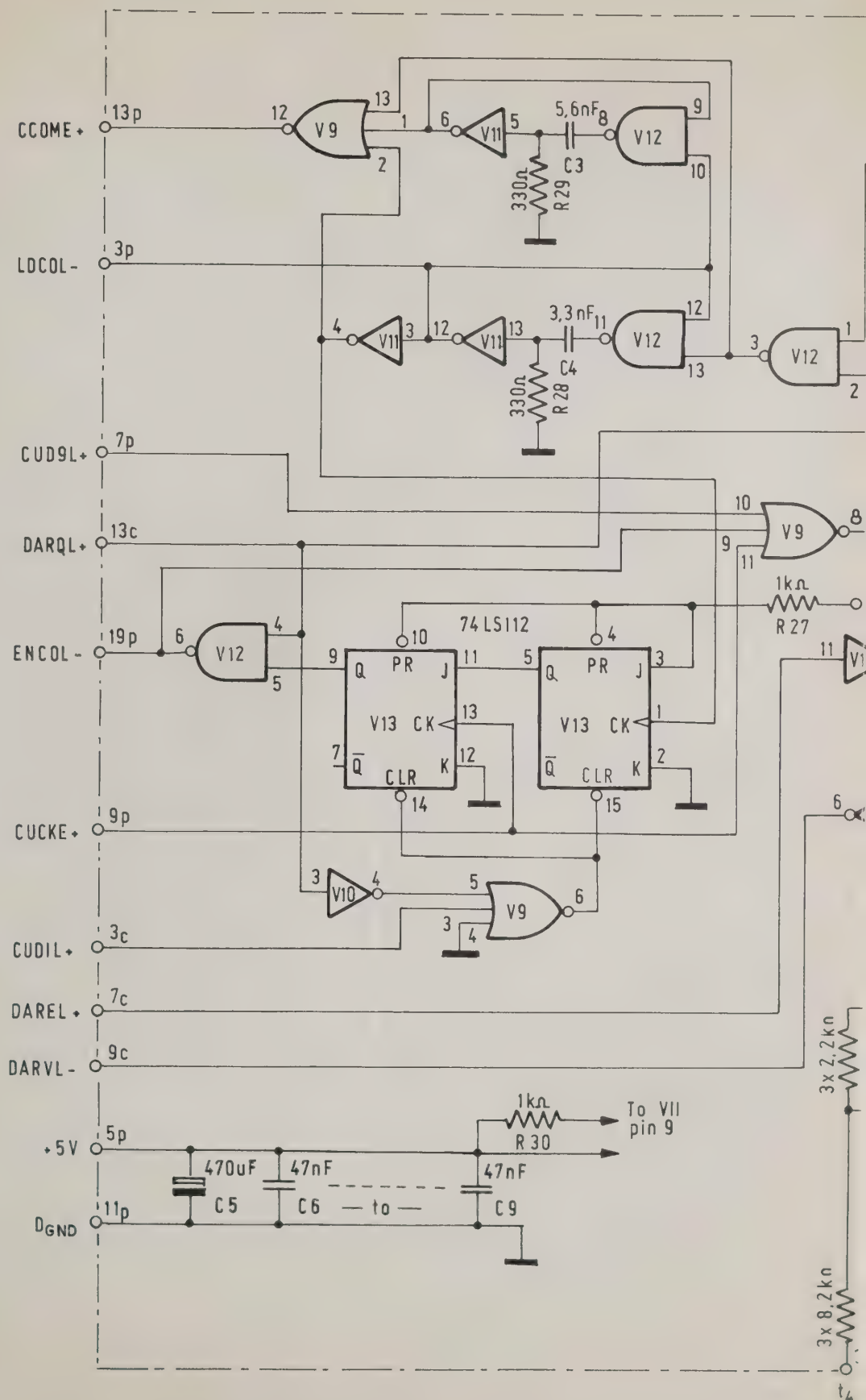
Inp. Amp. & Power Reg. Circuits

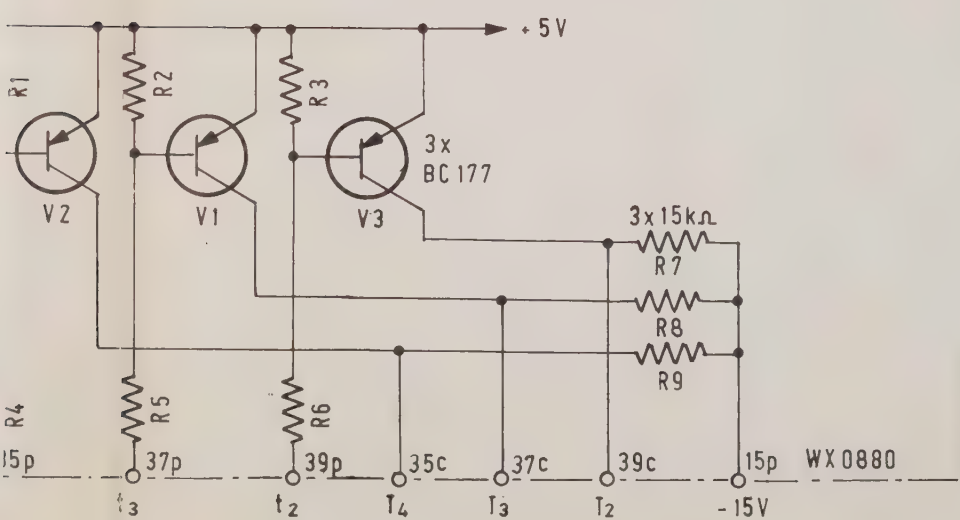
Type 5765

Title WI 0951, 52, 53, 56

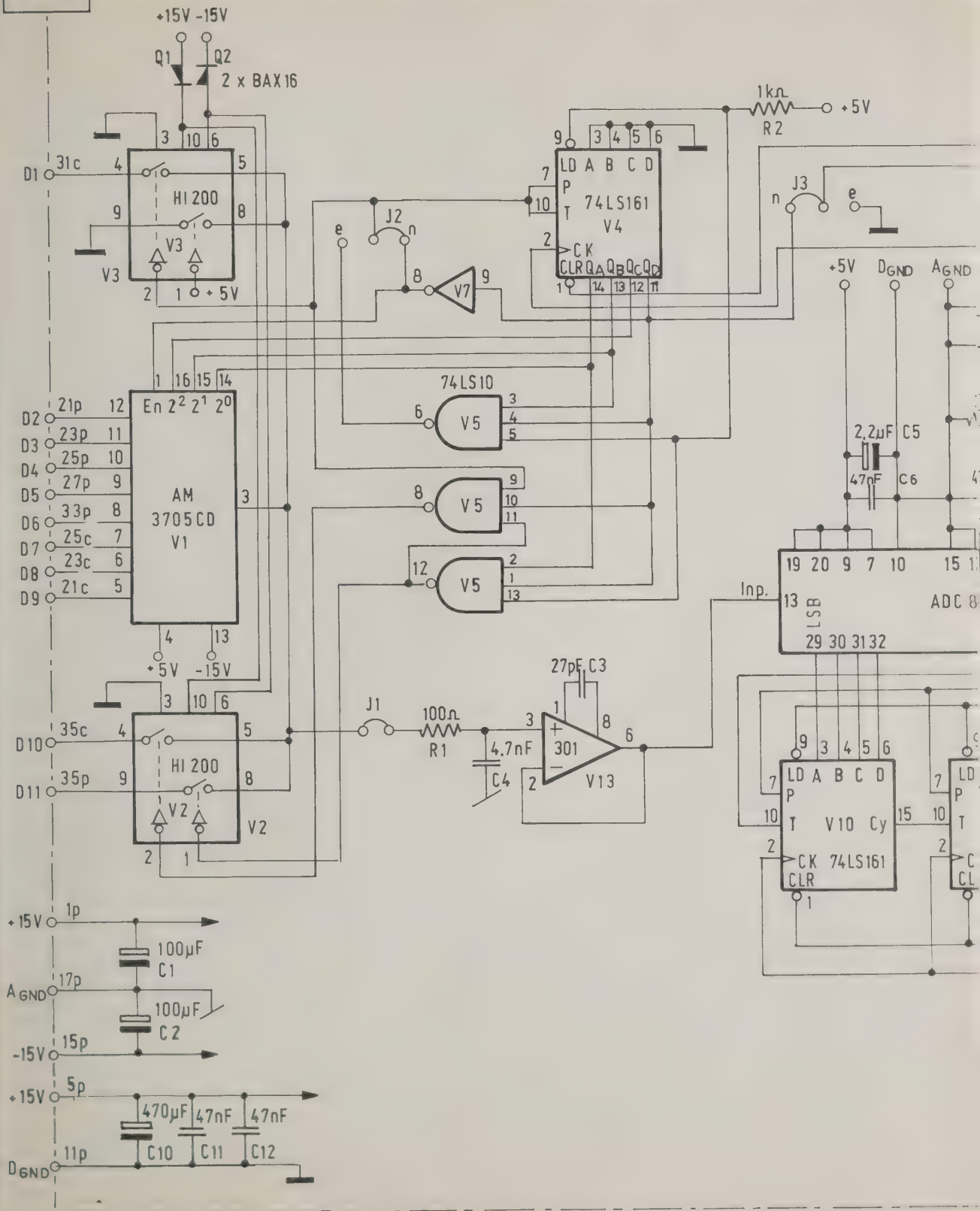
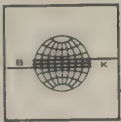
Drawn FLH/WS Date 14-6-77 Drawing no. WW 1700

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13p | DARQL +



13c CCOME +

7c DAREL+

9c¹ DARVL-
3p¹

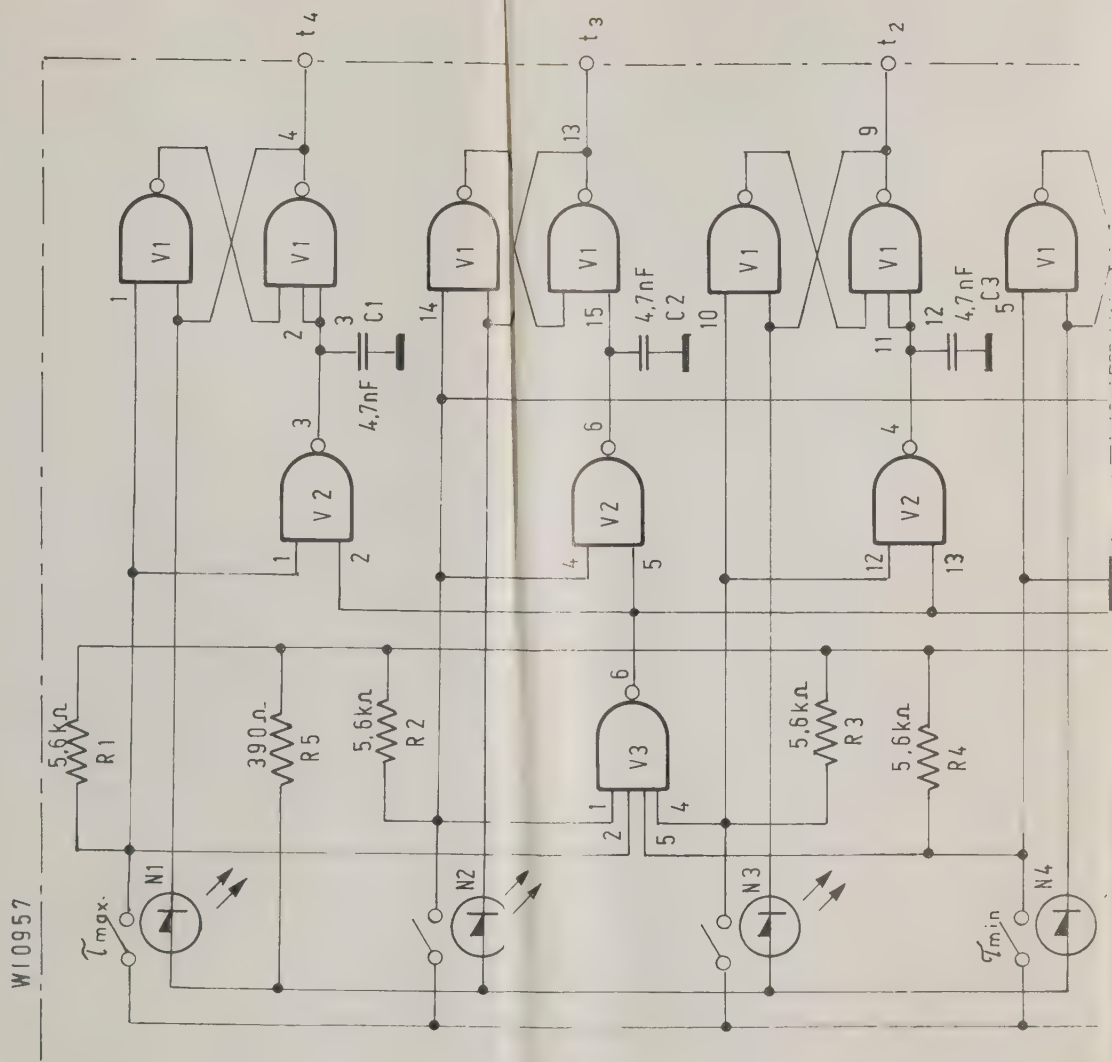
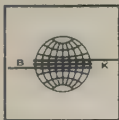
19c) ENCLOSURE

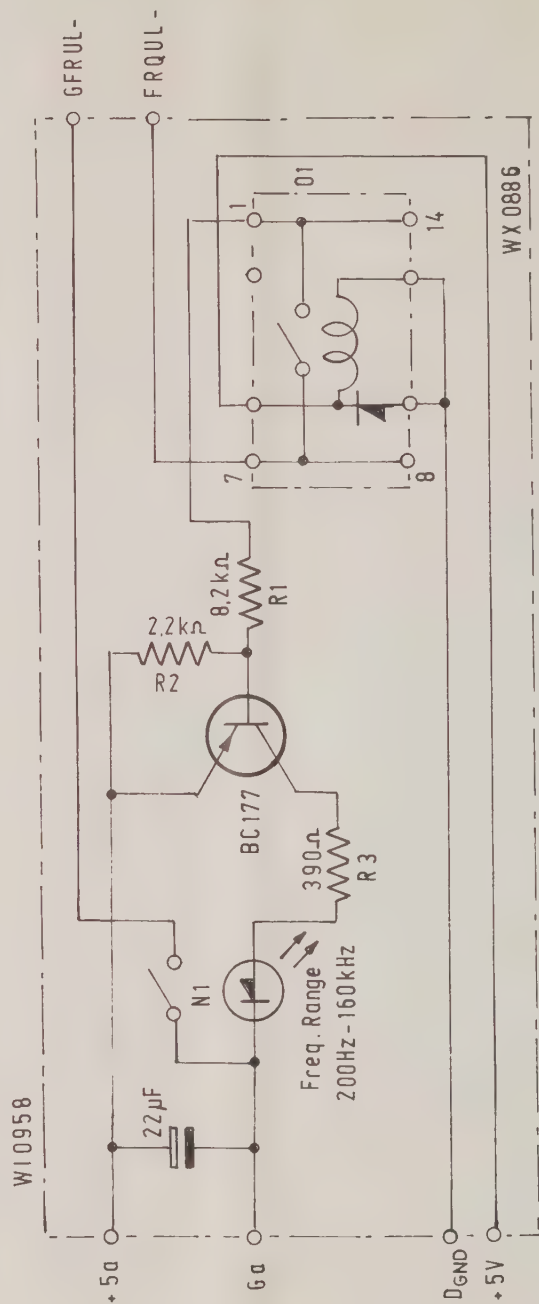
3c' LDCOL -

9p CUCKE

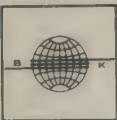
Type 5765

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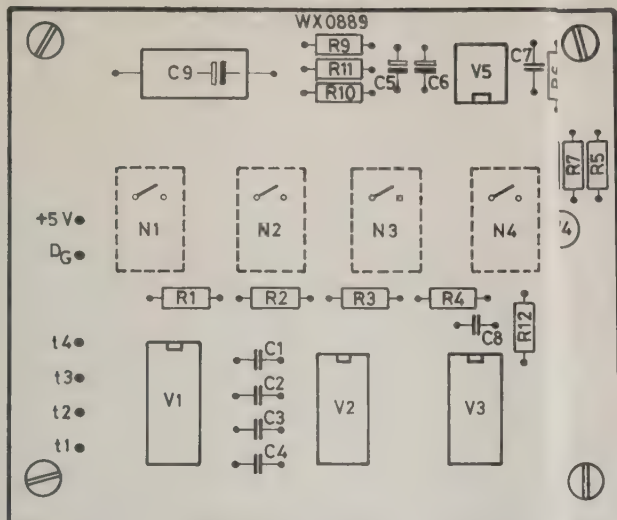




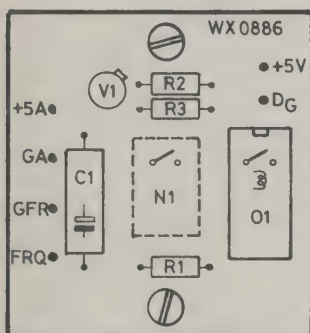
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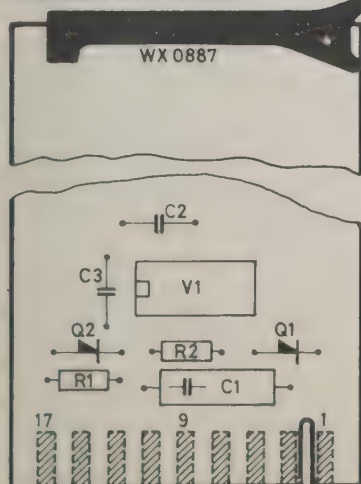
AVG. TIME CONTROL WI0957



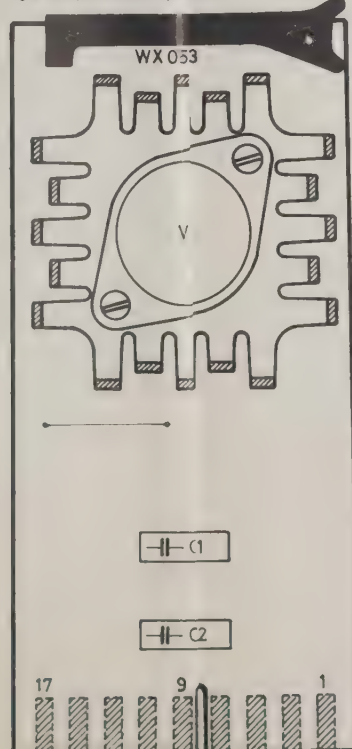
FREQ. RANGE CONTROL WI0958



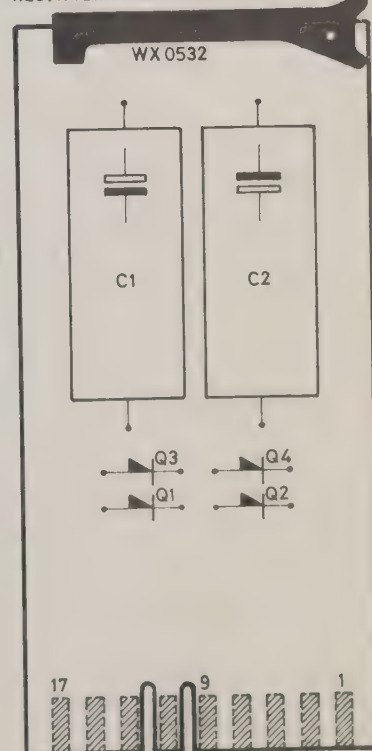
INPUT AMPLIFIER WI0953



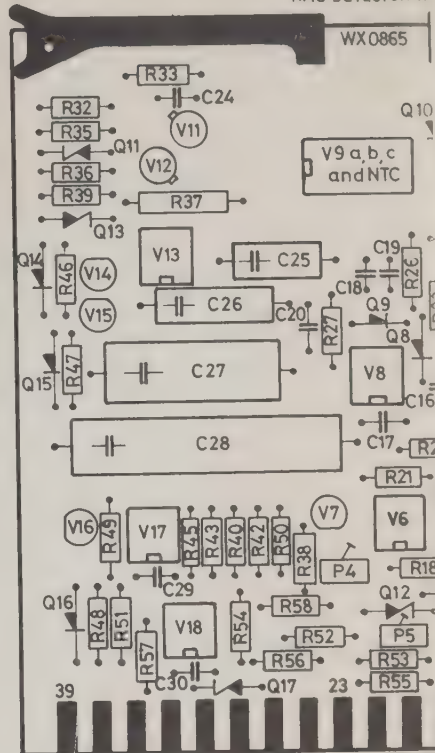
+5V REGULATOR WI0951



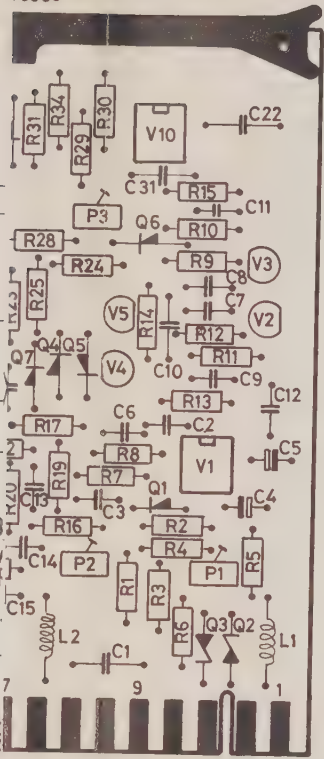
RECTIFIER WI0952



RMS DETECTOR W

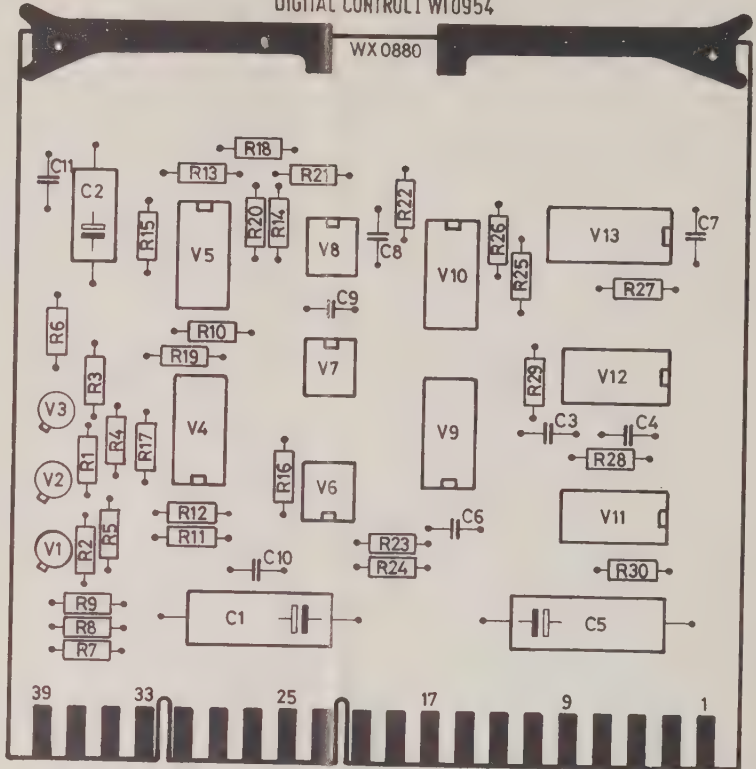


10950



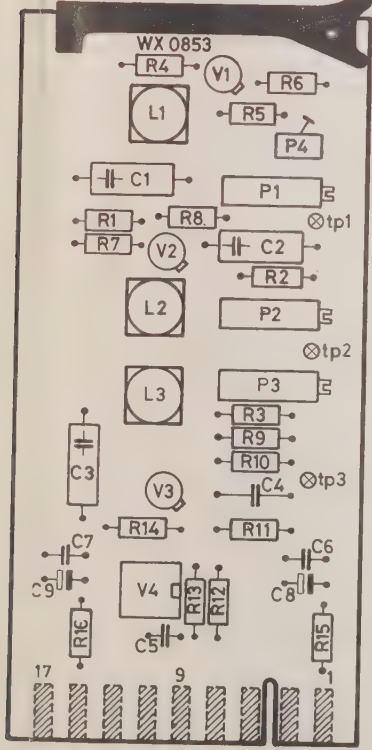
DIGITAL CONTROL I W10954

WX 0880



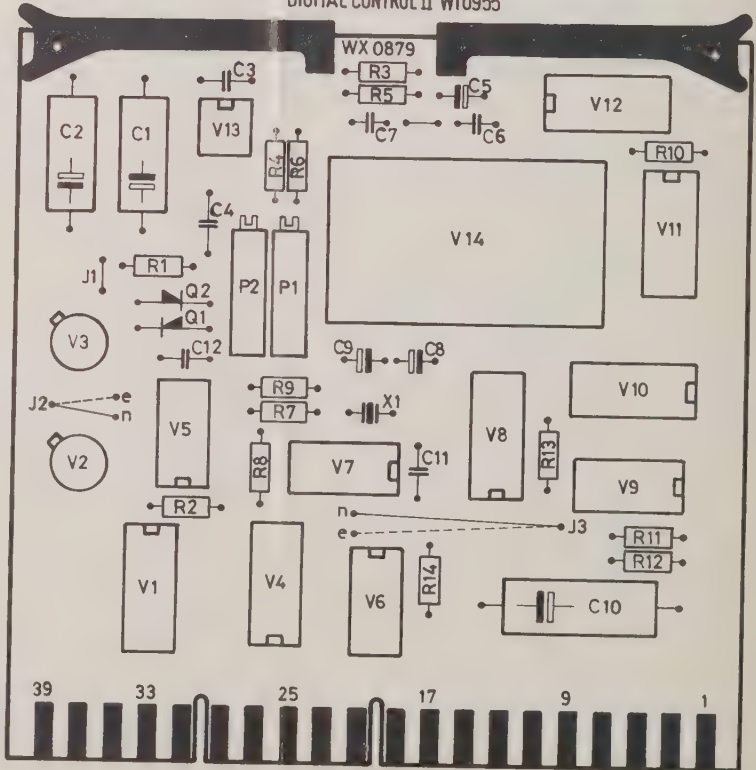
1/3 OCT. FILTER W10941 TO W10949

WX 0853



DIGITAL CONTROL II W10955

WX 0879

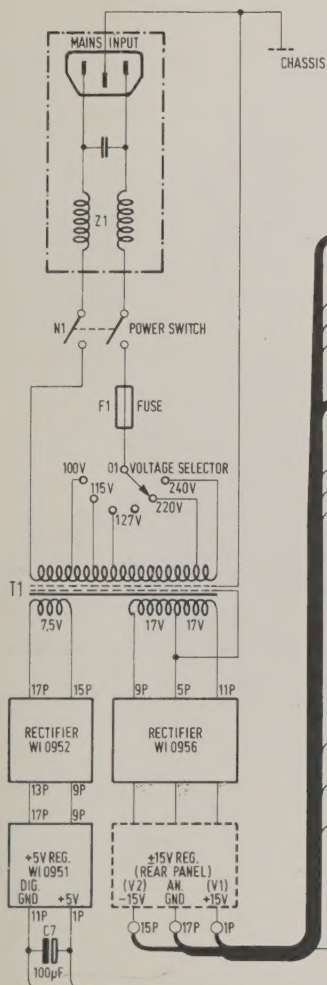


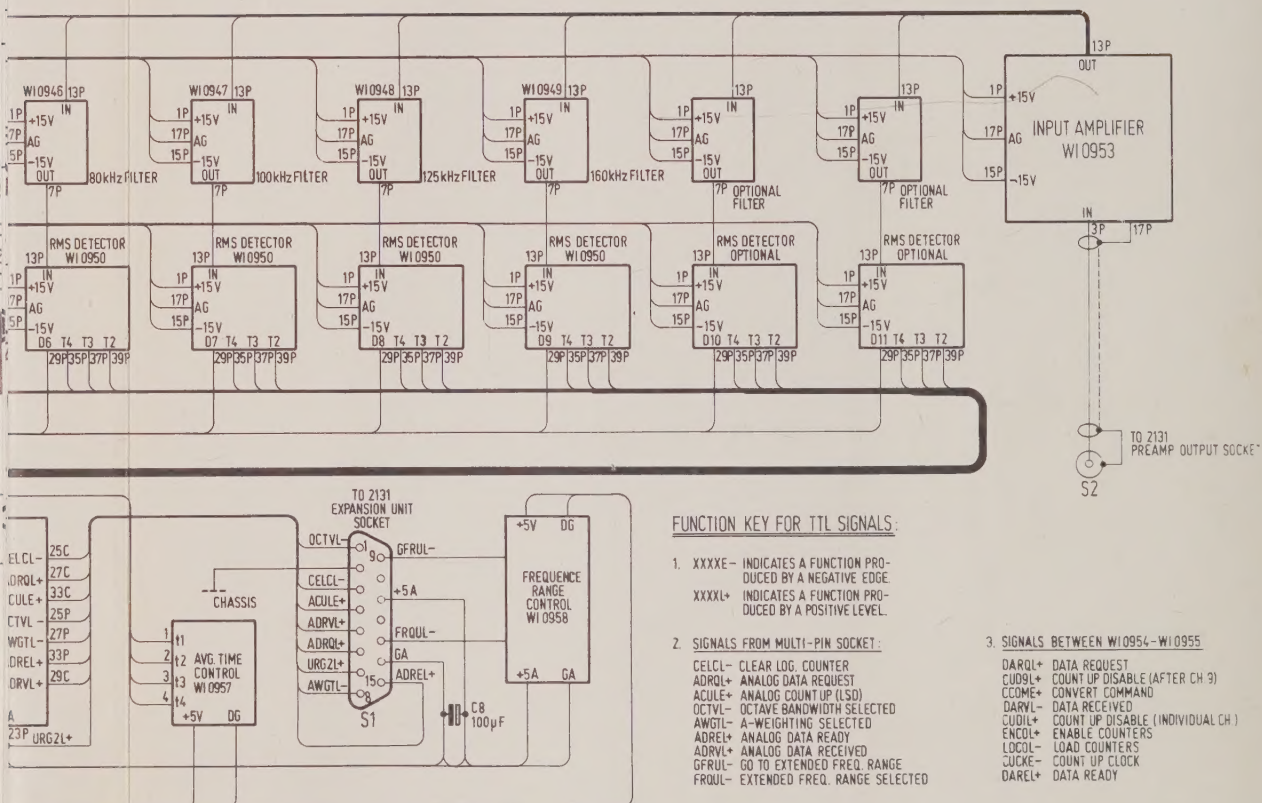
Title COMPONENT LOCATION DIAGRAM

TYPE 5765

Drawn FLH JOL Date 220877 Drawing no. WW1779

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Title **WIRING DIAGRAM FOR TYPE 5765**

Drawn **FLH** JOL Date **220877** Drawing no. **WW1780**

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At present, the following literature is available free of charge:

Power Spectral Density Measurements
Mechanical Vibration and Shock Measurements
Acoustic Noise Measurements
Standards, Formulae and Charts
Architectural Acoustics
Technical Review (4 times a year)

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